

# $2V_{RMS}$ DirectPath™, 112/106dB Audio Stereo DAC with 32-bit, 384kHz PCM Interface

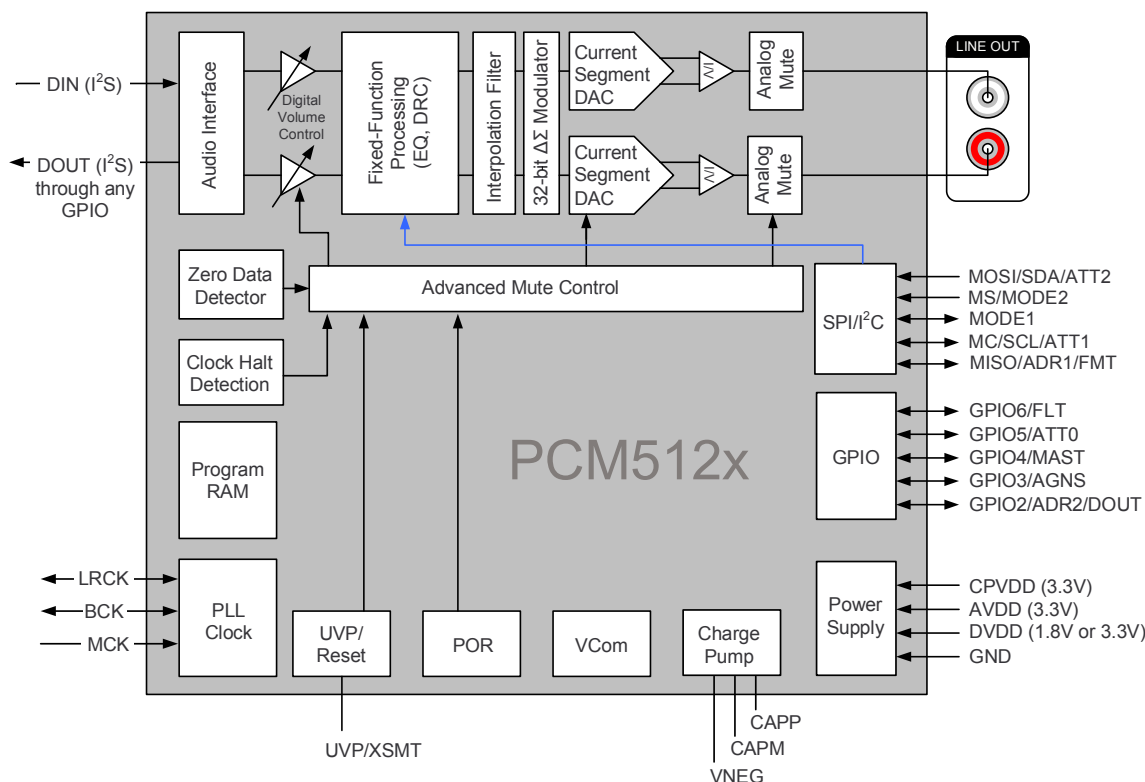
Check for Samples: [PCM5121](#), [PCM5122](#)

## FEATURES

- Register-Selectable Audio-Processing Functions
  - Dynamic Range Control (DRC)
  - Equalization (EQ)
  - Filtering
- Market-Leading Low Out-of-Band Noise
- Selectable Digital-Filter Latency and Performance
- No DC Blocking Capacitors Required
- Integrated Negative Charge Pump
- Internal Pop-Free Control For Sample-Rate Changes Or Clock Halts
- Intelligent Muting System; Soft Up or Down Ramp and Analog Mute For 120dB Mute SNR With Popless Operation

## Typical Performance (3.3V Power Supply)

| Parameter                                                                                                                | PCM5122                          | PCM5121 |
|--------------------------------------------------------------------------------------------------------------------------|----------------------------------|---------|
| SNR                                                                                                                      | 112dB                            | 106dB   |
| Dynamic Range                                                                                                            | 112dB                            | 106dB   |
| THD+N @ - 1dBFS                                                                                                          | -93dB                            | -92dB   |
| Full Scale Output                                                                                                        | 2.1V <sub>RMS</sub> (GND center) |         |
| Normal 8× Oversampling Digital Filter Latency: 20/f <sub>s</sub>                                                         |                                  |         |
| Low Latency 8× Oversampling Digital Filter Latency: 3.5/f <sub>s</sub>                                                   |                                  |         |
| Sampling Frequency                                                                                                       | 8kHz to 384kHz                   |         |
| System Clock Multiples (f <sub>SCk</sub> ): 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, 3072; up to 50 MHz |                                  |         |



**Figure 1. PCM512x Functional Block Diagram**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

System Two Cascade, Audio Precision are trademarks of Audio Precision.

DirectPath is a trademark of Texas, Instruments, Inc..

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012, Texas Instruments Incorporated



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## OTHER KEY FEATURES

- **Integrated High-Performance Audio PLL With BCK Reference To Generate SCK Internally**
- **Accepts 16-, 24-, And 32-Bit Audio Data**
- **PCM Data Formats: I<sup>2</sup>S, Left-Justified, Right-Justified, TDM**
- **SPI or I<sup>2</sup>C Control**
- **Software or Hardware Configuration**
- **Automatic Power-Save Mode When LRCK And BCK Are Deactivated**
- **3.3V Failsafe LVCMOS Digital Inputs**
- **Single Supply Operation:**
  - 3.3V Analog, 1.8V or 3.3V Digital
- **Integrated Power-On Reset**
- **Small 28-pin TSSOP Package**

## APPLICATIONS

- **A/V Receivers**
- **DVD, BD Players**
- **HDTV Receivers**
- **Applications Requiring 2V<sub>RMS</sub> Audio Output**

## DESCRIPTION

The PCM512x devices are a family of monolithic CMOS integrated circuits that include a stereo digital-to-analog converter and additional support circuitry in a small TSSOP package. The PCM512x uses the latest generation of TI's advanced segment-DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter.

Members of the PCM512x family integrate preset audio processing functions with programmable coefficients, allowing developers to change the characteristics of the interpolation filter, speaker EQ, dynamic range controls, and average volume control in their products.

The PCM512x provides 2.1V<sub>RMS</sub> ground centered outputs, allowing designers to eliminate DC blocking capacitors on the output, as well as external muting circuits traditionally associated with single supply line drivers.

The integrated line driver surpasses all other charge-pump based line drivers by supporting loads down to 1kΩ. By supporting loads down to 1kΩ, the PCM512x can essentially drive up to 10 products in parallel. (LCD TV, DVDR, AV Receivers etc).

The integrated PLL on the device removes the requirement for a system clock (commonly known as master clock), allowing a 3-wire I<sup>2</sup>S connection, along with reducing system EMI.

In addition, the PLL is completely programmable, allowing the device to become the I<sup>2</sup>S clock master and drive a DSP serial port as a slave. The PLL allows a non-standard clock (up to 50MHz) to be a source to generate the audio-related clock (such as 24.576MHz).

Intelligent clock error and PowerSense under voltage protection utilizes a two level mute system for pop-free performance. Upon clock error or system power failure, the device digitally attenuates the data (or last known good data), then mutes the analog circuit.

Compared with existing DAC technology, the PCM512x family offers up to 20dB lower out-of-band noise, reducing EMI and aliasing in downstream amplifiers/ADCs. (from traditional 100kHz OBN measurements all the way to 3MHz).

The PCM512x accepts industry-standard audio data formats with 16- to 32-bit data. Sample rates up to 384kHz are supported.

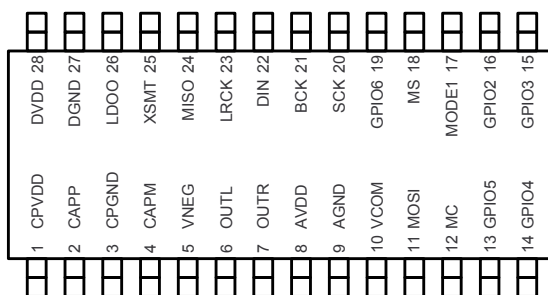
**Table 1. Differences Between PCM512x Devices**

| Part Number | Dynamic Range | SNR   | THD   |
|-------------|---------------|-------|-------|
| PCM5122     | 112dB         | 112dB | –93dB |
| PCM5121     | 106dB         | 106dB | –92dB |

## DEVICE INFORMATION

### PCM512x pin assignments-1 MODE1 tied DVDD : SPI mode

**PCM512x (top view)**



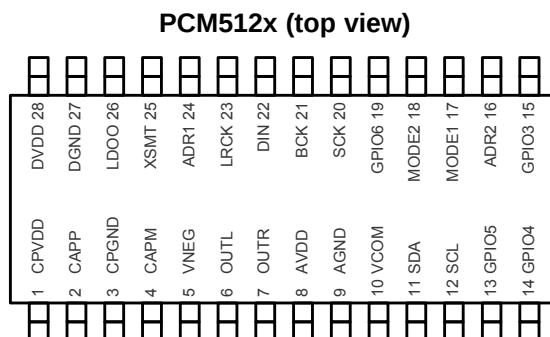
**Table 2. PCM512x SPI mode Terminal Functions**

| TERMINAL     |     | I/O | DESCRIPTION                                                                                                                                                                                                                 |
|--------------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME         | PIN |     |                                                                                                                                                                                                                             |
| CPVDD        | 1   | -   | Charge pump power supply, 3.3V                                                                                                                                                                                              |
| CAPP         | 2   | O   | Charge pump flying capacitor terminal for positive rail                                                                                                                                                                     |
| CPGND        | 3   | -   | Charge pump ground                                                                                                                                                                                                          |
| CAPM         | 4   | O   | Charge pump flying capacitor terminal for negative rail                                                                                                                                                                     |
| VNEG         | 5   | O   | Negative charge pump rail terminal for decoupling, -3.3V                                                                                                                                                                    |
| OUTL         | 6   | O   | Analog output from DAC left channel                                                                                                                                                                                         |
| OUTR         | 7   | O   | Analog output from DAC right channel                                                                                                                                                                                        |
| AVDD         | 8   | -   | Analog power supply, 3.3V                                                                                                                                                                                                   |
| AGND         | 9   | -   | Analog ground                                                                                                                                                                                                               |
| VCOM         | 10  | O   | VCOM output (Optional mode selected by register; default setting is VREF mode.) When in VREF mode (default), this pin ties to GND. When in VCOM mode, decoupling capacitor to GND is required.                              |
| MOSI         | 11  | I   | Input data for SPI <sup>(1)</sup>                                                                                                                                                                                           |
| MC           | 12  | I   | Input clock for SPI <sup>(1)</sup>                                                                                                                                                                                          |
| GPIO5        | 13  | I/O | General purpose digital input and output port                                                                                                                                                                               |
| GPIO4        | 14  | I/O | General purpose digital input and output port                                                                                                                                                                               |
| GPIO3        | 15  | I/O | General purpose digital input and output port                                                                                                                                                                               |
| GPIO2        | 16  | I/O | General purpose digital input and output port                                                                                                                                                                               |
| MODE1        | 17  | I   | Mode control selection pin <sup>(1)</sup>                                                                                                                                                                                   |
| MS (MODE2)   | 18  | I   | <ul style="list-style-type: none"> <li>MODE1=Low, MODE2=Low : Hardwired mode</li> <li>MODE1=Low, MODE2=High : I<sup>2</sup>C mode</li> <li>MODE1=High : SPI mode, MODE2 pin changes MS pin (chip select for SPI)</li> </ul> |
| GPIO6        | 19  | I/O | General purpose digital input and output port                                                                                                                                                                               |
| SCK          | 20  | I   | System clock input <sup>(1)</sup>                                                                                                                                                                                           |
| BCK          | 21  | I/O | Audio data bit clock input (slave) or output (master) <sup>(1)</sup>                                                                                                                                                        |
| DIN          | 22  | I   | Audio data input <sup>(1)</sup>                                                                                                                                                                                             |
| LRCK         | 23  | I/O | Audio data word clock input (slave) or output (master) <sup>(1)</sup>                                                                                                                                                       |
| MISO (GPIO1) | 24  | I/O | Primary output data for SPI readback<br>Secondary; general purpose digital input/output port controlled by register                                                                                                         |
| XSMT         | 25  | I   | Soft mute control <sup>(1)</sup> Soft mute (Low) / soft un-mute (High)                                                                                                                                                      |

(1) Failsafe LVCMOS Schmitt trigger input.

**Table 2. PCM512x SPI mode Terminal Functions (continued)**

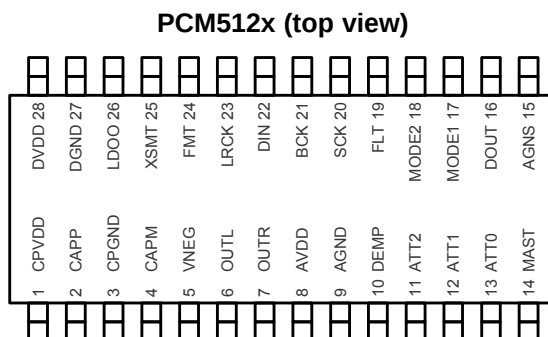
| TERMINAL |     | I/O | DESCRIPTION                                              |
|----------|-----|-----|----------------------------------------------------------|
| NAME     | PIN |     |                                                          |
| LDOO     | 26  | -   | Internal logic supply rail terminal for decoupling, 1.8V |
| DGND     | 27  | -   | Digital ground                                           |
| DVDD     | 28  | -   | Digital power supply, 3.3V or 1.8V                       |

**PCM512x pin assignments-2 MODE1 tied DGND and MODE2 tied DVDD : I<sup>2</sup>C mode**

**Table 3. PCM512x I<sup>2</sup>C mode Terminal Functions**

| TERMINAL |     | I/O | DESCRIPTIONS                                                                                                                                                                                                                |
|----------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME     | PIN |     |                                                                                                                                                                                                                             |
| CPVDD    | 1   | -   | Charge pump power supply, 3.3V                                                                                                                                                                                              |
| CAPP     | 2   | O   | Charge pump flying capacitor terminal for positive rail                                                                                                                                                                     |
| CPGND    | 3   | -   | Charge pump ground                                                                                                                                                                                                          |
| CAPM     | 4   | O   | Charge pump flying capacitor terminal for negative rail                                                                                                                                                                     |
| VNEG     | 5   | O   | Negative charge pump rail terminal for decoupling, -3.3V                                                                                                                                                                    |
| OUTL     | 6   | O   | Analog output from DAC left channel                                                                                                                                                                                         |
| OUTR     | 7   | O   | Analog output from DAC right channel                                                                                                                                                                                        |
| AVDD     | 8   | -   | Analog power supply, 3.3V                                                                                                                                                                                                   |
| AGND     | 9   | -   | Analog ground                                                                                                                                                                                                               |
| VCOM     | 10  | I   | VCOM output (Optional mode selected by register; default setting is VREF mode.) When in VREF mode (default), this pin ties to GND. When in VCOM mode, decoupling capacitor to GND is required.                              |
| SDA      | 11  | I/O | Input data for I <sup>2</sup> C <sup>(1)(2)</sup>                                                                                                                                                                           |
| SCL      | 12  | I   | Input clock for I <sup>2</sup> C <sup>(2)</sup>                                                                                                                                                                             |
| GPIO5    | 13  | I/O | General purpose digital input and output port                                                                                                                                                                               |
| GPIO4    | 14  | I/O | General purpose digital input and output port                                                                                                                                                                               |
| GPIO3    | 15  | I/O | General purpose digital input and output port                                                                                                                                                                               |
| ADR2     | 16  | I   | 2nd LSB address select bit for I <sup>2</sup> C                                                                                                                                                                             |
| MODE1    | 17  | I   | Mode-control selection pins <sup>(2)</sup>                                                                                                                                                                                  |
| MODE2    | 18  | I   | <ul style="list-style-type: none"> <li>MODE1=Low, MODE2=Low : Hardwired mode</li> <li>MODE1=Low, MODE2=High : I<sup>2</sup>C mode</li> <li>MODE1=High : SPI mode, MODE2 pin changes MS pin (chip select for SPI)</li> </ul> |
| GPIO6    | 19  | I/O | General purpose digital input and output port                                                                                                                                                                               |
| SCK      | 20  | I   | System clock input <sup>(2)</sup>                                                                                                                                                                                           |
| BCK      | 21  | I/O | Audio data bit clock input (slave) or output (master) <sup>(2)</sup>                                                                                                                                                        |
| DIN      | 22  | I   | Audio data input <sup>(2)</sup>                                                                                                                                                                                             |
| LRCK     | 23  | I/O | Audio data word clock input (slave) or output (master) <sup>(2)</sup>                                                                                                                                                       |
| ADR1     | 24  | I   | LSB address select bit for I <sup>2</sup> C                                                                                                                                                                                 |
| XSMT     | 25  | I   | Soft mute control : Soft mute (Low) / soft un-mute (High) <sup>(2)</sup>                                                                                                                                                    |
| LDOO     | 26  | -   | Internal logic supply rail terminal for decoupling, 1.8V                                                                                                                                                                    |
| DGND     | 27  | -   | Digital ground                                                                                                                                                                                                              |
| DVDD     | 28  | -   | Digital power supply, 3.3V or 1.8V                                                                                                                                                                                          |

- (1) Open-drain configuration in out mode.  
(2) Failsafe LVCMOS Schmitt trigger input.

## PCM512x pin assignments-3 MODE1 tied DGND and MODE2 tied DGND : Hardwired mode



The H/W mode has digital gain and attenuation level control by decoding external ATT2 (11 pin), ATT1 (12 pin), and ATT0 (pin 13). Table 1 shows the pins used to set gain and attenuation levels.

**Table 4. Gain and Attenuation in Hardware Mode**

| ATT pin condition (ATT2 : ATT1 : ATT0) | Gain and Attenuation level |
|----------------------------------------|----------------------------|
| ( 0 0 0 )                              | 0 dB                       |
| ( 0 0 1 )                              | + 3 dB                     |
| ( 0 1 0 )                              | + 6 dB                     |
| ( 0 1 1 )                              | + 9 dB                     |
| ( 1 0 0 )                              | + 12 dB                    |
| ( 1 0 1 )                              | + 15 dB                    |
| ( 1 1 0 )                              | - 6 dB                     |
| ( 1 1 1 )                              | - 3 dB                     |

**Table 5. PCM512x Hardwired mode Terminal Functions**

| Terminal |     | I/O | Description                                                                                            |
|----------|-----|-----|--------------------------------------------------------------------------------------------------------|
| Name     | Pin |     |                                                                                                        |
| CPVDD    | 1   | -   | Charge pump power supply, 3.3V                                                                         |
| CAPP     | 2   | O   | Charge pump flying capacitor terminal for positive rail                                                |
| CPGND    | 3   | -   | Charge pump ground                                                                                     |
| CAPM     | 4   | O   | Charge pump flying capacitor terminal for negative rail                                                |
| VNEG     | 5   | O   | Negative charge pump rail terminal for decoupling, -3.3V                                               |
| OUTL     | 6   | O   | Analog output from DAC left channel                                                                    |
| OUTR     | 7   | O   | Analog output from DAC right channel                                                                   |
| AVDD     | 8   | -   | Analog power supply, 3.3V                                                                              |
| AGND     | 9   | -   | Analog ground                                                                                          |
| DEMP     | 10  | I   | De-emphasis control for 44.1kHz sampling rate <sup>(1)</sup> : Off (Low) / On (High)                   |
| ATT2     | 11  | I   | Digital gain and attenuation control pin <sup>(1)</sup>                                                |
| ATT1     | 12  | I   | Digital gain and attenuation control pin <sup>(1)</sup>                                                |
| ATT0     | 13  | I   | Digital gain and attenuation control pin                                                               |
| MAST     | 14  | I   | I <sup>2</sup> S Master clock select pin : Master (High) BCK/LRCK outputs, Slave (Low) BCK/LRCK inputs |
| AGNS     | 15  | I   | Analog gain selector : 0dB 2V <sub>RMS</sub> output (Low), -6dB 1V <sub>RMS</sub> output (High)        |
| GPO      | 16  | O   | General Purpose Output (Low level)                                                                     |

(1) Failsafe LVCMOS Schmitt trigger input.

**Table 5. PCM512x Hardwired mode Terminal Functions (continued)**

| Terminal |     | I/O | Description                                                                                                                                                                                                                                                               |
|----------|-----|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name     | Pin |     |                                                                                                                                                                                                                                                                           |
| MODE1    | 17  | I   | Mode-control selection pins <sup>(2)</sup><br><ul style="list-style-type: none"> <li>MODE1=Low, MODE2=Low : Hardwired mode</li> <li>MODE1=Low, MODE2=High : I<sup>2</sup>C mode</li> <li>MODE1=High : SPI mode, MODE2 pin changes MS pin (chip select for SPI)</li> </ul> |
| MODE2    | 18  | I   |                                                                                                                                                                                                                                                                           |
| FLT      | 19  | I   | Filter select : Normal latency (Low) / Low latency (High)                                                                                                                                                                                                                 |
| SCK      | 20  | I   | System clock input <sup>(2)</sup>                                                                                                                                                                                                                                         |
| BCK      | 21  | I/O | Audio data bit clock input <sup>(2)</sup>                                                                                                                                                                                                                                 |
| DIN      | 22  | I   | Audio data input <sup>(2)</sup>                                                                                                                                                                                                                                           |
| LRCK     | 23  | I/O | Audio data word clock input <sup>(2)</sup>                                                                                                                                                                                                                                |
| FMT      | 24  | I   | Audio format selection : I <sup>2</sup> S (Low) / Left justified (High)                                                                                                                                                                                                   |
| XSMT     | 25  | I   | Soft mute control : Soft mute (Low) / soft un-mute (High) <sup>(2)</sup>                                                                                                                                                                                                  |
| LDOO     | 26  | -   | Internal logic supply rail terminal for decoupling, 1.8V                                                                                                                                                                                                                  |
| DGND     | 27  | -   | Digital ground                                                                                                                                                                                                                                                            |
| DVDD     | 28  | -   | Digital power supply, 3.3V or 1.8V                                                                                                                                                                                                                                        |

(2) Failsafe LVCMOS Schmitt trigger input.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

|                             |                                                                             | VALUE        | UNIT |
|-----------------------------|-----------------------------------------------------------------------------|--------------|------|
| Supply Voltage              | AVDD, CPVDD, DVDD                                                           | –0.3 to 3.9  | V    |
|                             | LDOO with DVDD at 1.8V (See <a href="#">Typical Applications Circuits</a> ) | –0.3 to 2.25 |      |
| Digital Input Voltage       | DVDD at 1.8V                                                                | –0.3 to 2.25 |      |
|                             | DVDD at 3.3V                                                                | –0.3 to 3.9  |      |
| Analog Input Voltage        |                                                                             | –0.3 to 3.9  | °C   |
| Operating Temperature Range |                                                                             | –25 to 85    |      |
| Storage Temperature Range   |                                                                             | –65 to 150   |      |

## THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER     |          | TEST CONDITIONS | MIN | TYP  | MAX | UNIT |
|---------------|----------|-----------------|-----|------|-----|------|
| $\theta_{JA}$ | Theta JA | High K          |     | 72.2 |     | °C/W |
| $\theta_{JC}$ | Theta JC | Top             |     | 17.5 |     |      |
| $\theta_{JB}$ | Theta JB |                 |     | 35.0 |     |      |
| $\Psi_{JT}$   | Psi JT   |                 |     | 0.4  |     |      |
| $\Psi_{JB}$   | Psi JB   |                 |     | 34.5 |     |      |

## ELECTRICAL CHARACTERISTICS

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{V}$ ,  $f_s = 48\text{kHz}$ , system clock =  $512f_s$  and 24-bit data unless otherwise noted.

| PARAMETER                            |                                                   | TEST CONDITIONS                                 | MIN                                                                                              | TYP | MAX | UNIT |
|--------------------------------------|---------------------------------------------------|-------------------------------------------------|--------------------------------------------------------------------------------------------------|-----|-----|------|
|                                      | Resolution                                        |                                                 | 16                                                                                               | 24  | 32  | Bits |
| Data Format (PCM Mode)               |                                                   |                                                 |                                                                                                  |     |     |      |
|                                      | Audio data interface format                       |                                                 | I <sup>2</sup> S, left justified, right justified and TDM                                        |     |     |      |
|                                      | Audio data bit length                             |                                                 | 16, 24, 32-bit acceptable                                                                        |     |     |      |
|                                      | Audio data format                                 |                                                 | MSB First, 2s Complement                                                                         |     |     |      |
| f <sub>S</sub> <sup>(1)</sup>        | Sampling frequency                                |                                                 | 8                                                                                                |     | 384 | kHz  |
| Clocks                               |                                                   |                                                 |                                                                                                  |     |     |      |
|                                      | System clock frequency                            |                                                 | 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072 f <sub>SCK</sub> , up to 50Mhz |     |     |      |
|                                      | PLL Input Frequency (SCL Clock Frequency 400 kHz) | Clock divider uses fractional divide D > 0, P=1 | 6.7                                                                                              |     | 20  | MHz  |
|                                      |                                                   | Clock divider uses integer divide D = 0, P=1    | 1                                                                                                |     | 20  | MHz  |
| Digital Input/Output                 |                                                   |                                                 |                                                                                                  |     |     |      |
| Logic Family: 3.3V LVCMOS compatible |                                                   |                                                 |                                                                                                  |     |     |      |
| V <sub>IH</sub>                      | Input logic level                                 |                                                 | 0.7×DV <sub>DD</sub>                                                                             |     |     | V    |
| V <sub>IL</sub>                      |                                                   |                                                 | 0.3×DV <sub>DD</sub>                                                                             |     |     |      |
| I <sub>IH</sub>                      | Input logic current                               | V <sub>IN</sub> = V <sub>DD</sub>               | 10                                                                                               |     |     | μA   |
| I <sub>IL</sub>                      |                                                   | V <sub>IN</sub> = 0V                            | −10                                                                                              |     |     |      |
| V <sub>OH</sub>                      | Output logic level                                | I <sub>OH</sub> = −4mA                          | 0.8×DV <sub>DD</sub>                                                                             |     |     | V    |
| V <sub>OL</sub>                      |                                                   | I <sub>OL</sub> = 4mA                           | 0.22×DV <sub>D</sub> <sub>D</sub>                                                                |     |     |      |
| Logic Family 1.8V LVCMOS compatible  |                                                   |                                                 |                                                                                                  |     |     |      |
| V <sub>IH</sub>                      | Input logic level                                 |                                                 | 0.7×DV <sub>DD</sub>                                                                             |     |     | V    |
| V <sub>IL</sub>                      |                                                   |                                                 | 0.3×DV <sub>DD</sub>                                                                             |     |     |      |
| I <sub>IH</sub>                      | Input logic current                               | V <sub>IN</sub> = V <sub>DD</sub>               | 10                                                                                               |     |     | μA   |
| I <sub>IL</sub>                      |                                                   | V <sub>IN</sub> = 0V                            | −10                                                                                              |     |     |      |
| V <sub>OH</sub>                      | Output logic level                                | I <sub>OH</sub> = −2mA                          | 0.8×DV <sub>DD</sub>                                                                             |     |     | V    |
| V <sub>OL</sub>                      |                                                   | I <sub>OL</sub> = 2mA                           | 0.22×DV <sub>D</sub> <sub>D</sub>                                                                |     |     |      |

(1) One sample time  $t_s$  defined as the reciprocal of the sampling frequency.  $1t_s = 1/f_s$

**ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{V}$ ,  $f_S = 48\text{kHz}$ , system clock =  $512f_S$  and 24-bit data unless otherwise noted.

| PARAMETER                                                                                               |  | TEST CONDITIONS                         | MIN       | TYP       | MAX | UNIT |
|---------------------------------------------------------------------------------------------------------|--|-----------------------------------------|-----------|-----------|-----|------|
| <b>Dynamic Performance (PCM Mode)<sup>(2)(3)</sup> (Values shown for two devices PCM5122 / PCM5121)</b> |  |                                         |           |           |     |      |
| THD+N at -1 dB <sup>(3)</sup>                                                                           |  | $f_S = 48\text{kHz}$                    | -93 / -92 | -83 / -82 |     | dB   |
|                                                                                                         |  | $f_S = 96\text{kHz}$                    | -93 / -92 |           |     |      |
|                                                                                                         |  | $f_S = 192\text{kHz}$                   | -93 / -92 |           |     |      |
| Dynamic range <sup>(3)</sup>                                                                            |  | EIAJ, A-weighted, $f_S = 48\text{kHz}$  | 106 / 100 | 112 / 106 |     |      |
|                                                                                                         |  | EIAJ, A-weighted, $f_S = 96\text{kHz}$  |           | 112 / 106 |     |      |
|                                                                                                         |  | EIAJ, A-weighted, $f_S = 192\text{kHz}$ |           | 112 / 106 |     |      |
| Signal-to-noise ratio <sup>(3)</sup>                                                                    |  | EIAJ, A-weighted, $f_S = 48\text{kHz}$  |           | 112 / 106 |     |      |
|                                                                                                         |  | EIAJ, A-weighted, $f_S = 96\text{kHz}$  |           | 112 / 106 |     |      |
|                                                                                                         |  | EIAJ, A-weighted, $f_S = 192\text{kHz}$ |           | 112 / 106 |     |      |
| Signal to noise ratio with analog mute <sup>(3)(4)</sup>                                                |  | EIAJ, A-weighted, $f_S = 48\text{kHz}$  | 113       | 123       |     |      |
|                                                                                                         |  | EIAJ, A-weighted, $f_S = 96\text{kHz}$  | 113       | 123       |     |      |
|                                                                                                         |  | EIAJ, A-weighted, $f_S = 192\text{kHz}$ | 113       | 123       |     |      |
| Channel Separation                                                                                      |  | $f_S = 48\text{kHz}$                    | 100 / 95  | 109 / 103 |     |      |
|                                                                                                         |  | $f_S = 96\text{kHz}$                    | 100 / 95  | 109 / 103 |     |      |
|                                                                                                         |  | $f_S = 192\text{kHz}$                   | 100 / 95  | 109 / 103 |     |      |

(2) Filter condition: THD+N: 20Hz HPF, 20kHz AES17 LPF Dynamic range: 20Hz HPF, 20kHz AES17 LPF, A-weighted Signal-to-noise ratio: 20Hz HPF, 20kHz AES17 LPF, A-weighted Channel separation: 20Hz HPF, 20kHz AES17 LPF Analog performance specifications are measured using the System Two Cascade™ audio measurement system by Audio Precision™ in the RMS mode.

(3) Output load is 10kΩ, with 470Ω output resistor and a 2.2nF shunt capacitor (see recommended output filter).

(4) Assert XSMT or both L-ch and R-ch PCM data are BPZ

## ELECTRICAL CHARACTERISTICS (continued)

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{V}$ ,  $f_s = 48\text{kHz}$ , system clock =  $512f_s$  and 24-bit data unless otherwise noted.

| PARAMETER                                              | TEST CONDITIONS | MIN       | TYP       | MAX          | UNIT       |
|--------------------------------------------------------|-----------------|-----------|-----------|--------------|------------|
| <b>Analog Output</b>                                   |                 |           |           |              |            |
| Output voltage                                         |                 |           | 2.1       |              | $V_{RMS}$  |
| Gain error                                             |                 | –6        | $\pm 2.0$ | 6            | % of FSR   |
| Gain mismatch, channel-to-channel                      |                 | –6        | $\pm 0.5$ | 6            | % of FSR   |
| Bipolar zero error                                     | At bipolar zero | –5        | $\pm 1.0$ | 5            | mV         |
| Load impedance                                         |                 | 1         |           |              | k $\Omega$ |
| <b>Filter Characteristics–1: Normal (8x)</b>           |                 |           |           |              |            |
| Pass band                                              |                 |           |           | $0.45f_s$    |            |
| Stop band                                              |                 | $0.55f_s$ |           |              |            |
| Stop band attenuation                                  |                 | –60       |           |              | dB         |
| Pass-band ripple                                       |                 |           |           | $\pm 0.02$   |            |
| Delay time                                             |                 |           | $20t_s$   |              | s          |
| <b>Filter Characteristics–2: Low Latency (8x)</b>      |                 |           |           |              |            |
| Pass band                                              |                 |           |           | $0.47f_s$    |            |
| Stop band                                              |                 | $0.55f_s$ |           |              |            |
| Stop band attenuation                                  |                 | –52       |           |              | dB         |
| Pass-band ripple                                       |                 |           |           | $\pm 0.0001$ |            |
| Delay time                                             |                 |           | $3.5t_s$  |              | s          |
| <b>Filter Characteristics–3: Asymmetric FIR (8x)</b>   |                 |           |           |              |            |
| Pass band                                              |                 |           |           | $0.40f_s$    |            |
| Stop band                                              |                 | $0.72f_s$ |           |              |            |
| Stop band attenuation                                  |                 | –52       |           |              | dB         |
| Pass-band ripple                                       |                 |           |           | $\pm 0.05$   |            |
| Delay time                                             |                 |           | $1.2t_s$  |              | s          |
| <b>Filter Characteristics–4: High-Attenuation (8x)</b> |                 |           |           |              |            |
| Pass band                                              |                 |           |           | $0.45f_s$    |            |
| Stop band                                              |                 | $0.45f_s$ |           |              |            |
| Stop band attenuation                                  |                 |           | –100      |              | dB         |
| Pass-band ripple                                       |                 |           |           | $\pm 0.0005$ |            |
| Delay time                                             |                 |           | $33.7t_s$ |              | s          |

**ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{V}$ ,  $f_S = 48\text{kHz}$ , system clock =  $512f_S$  and 24-bit data unless otherwise noted.

| PARAMETER                        |                                                    | TEST CONDITIONS                                    | MIN  | TYP   | MAX   | UNIT |
|----------------------------------|----------------------------------------------------|----------------------------------------------------|------|-------|-------|------|
| <b>Power Supply Requirements</b> |                                                    |                                                    |      |       |       |      |
| $DV_{DD}$                        | Digital supply voltage                             | Target $DV_{DD} = 1.8\text{V}$                     | 1.65 | 1.8   | 1.95  | VDC  |
| $DV_{DD}$                        | Digital supply voltage                             | Target $DV_{DD} = 3.3\text{V}$                     | 3.0  | 3.3   | 3.6   | VDC  |
| $AV_{DD}$                        | Analog supply voltage                              |                                                    | 3.0  | 3.3   | 3.6   |      |
| $CPV_{DD}$                       | Charge-pump supply voltage                         |                                                    | 3.0  | 3.3   | 3.6   |      |
| $I_{DD}$                         | $DV_{DD}$ supply current at $1.8\text{V}^{(5)}$    | $f_S = 48\text{kHz}$ , Input is Bipolar Zero data  |      | 11    | 14    | mA   |
|                                  |                                                    | $f_S = 96\text{kHz}$ , Input is Bipolar Zero data  |      | 12    |       |      |
|                                  |                                                    | $f_S = 192\text{kHz}$ , Input is Bipolar Zero data |      | 14    |       |      |
| $I_{DD}$                         | $DV_{DD}$ supply current at $1.8\text{V}^{(6)}$    | $f_S = 48\text{kHz}$ , Input is 1kHz -1dBFS data   |      | 11    | 14    | mA   |
|                                  |                                                    | $f_S = 96\text{kHz}$ , Input is 1kHz -1dBFS data   |      | 12    |       |      |
|                                  |                                                    | $f_S = 192\text{kHz}$ , Input is 1kHz -1dBFS data  |      | 14    |       |      |
| $I_{DD}$                         | $DV_{DD}$ supply current at $1.8\text{V}^{(7)}$    | $f_S = \text{N/A}$ , Power Down Mode               |      | 0.3   | 0.6   | mA   |
| $I_{DD}$                         | $DV_{DD}$ supply current at $3.3\text{V}^{(5)}$    | $f_S = 48\text{kHz}$ , Input is Bipolar Zero data  |      | 12    | 15    | mA   |
|                                  |                                                    | $f_S = 96\text{kHz}$ , Input is Bipolar Zero data  |      | 13    |       |      |
|                                  |                                                    | $f_S = 192\text{kHz}$ , Input is Bipolar Zero data |      | 15    |       |      |
| $I_{DD}$                         | $DV_{DD}$ supply current at $3.3\text{V}^{(6)}$    | $f_S = 48\text{kHz}$ , Input is 1kHz -1dBFS data   |      | 12    | 15    | mA   |
|                                  |                                                    | $f_S = 96\text{kHz}$ , Input is 1kHz -1dBFS data   |      | 13    |       |      |
|                                  |                                                    | $f_S = 192\text{kHz}$ , Input is 1kHz -1dBFS data  |      | 15    |       |      |
| $I_{DD}$                         | $DV_{DD}$ supply current at $3.3\text{V}^{(7)}$    | $f_S = \text{N/A}$ , Power Down Mode               |      | 0.5   | 0.8   | mA   |
| $I_{CC}$                         | $AV_{DD} / CPV_{DD}$ Supply Current <sup>(5)</sup> | $f_S = 48\text{kHz}$ , Input is Bipolar Zero data  |      | 11    | 16    | mA   |
|                                  |                                                    | $f_S = 96\text{kHz}$ , Input is Bipolar Zero data  |      | 11    |       |      |
|                                  |                                                    | $f_S = 192\text{kHz}$ , Input is Bipolar Zero data |      | 11    |       |      |
| $I_{CC}$                         | $AV_{DD} / CPV_{DD}$ Supply Current <sup>(6)</sup> | $f_S = 48\text{kHz}$ , Input is 1kHz -1dBFS data   |      | 24    | 32    | mA   |
|                                  |                                                    | $f_S = 96\text{kHz}$ , Input is 1kHz -1dBFS data   |      | 24    |       |      |
|                                  |                                                    | $f_S = 192\text{kHz}$ , Input is 1kHz -1dBFS data  |      | 24    |       |      |
| $I_{CC}$                         | $AV_{DD} / CPV_{DD}$ Supply Current <sup>(7)</sup> | $f_S = \text{N/A}$ , Power Down Mode               |      | 0.2   | 0.4   | mA   |
|                                  | Power Dissipation, $DV_{DD} = 1.8\text{V}^{(5)}$   | $f_S = 48\text{kHz}$ , Input is Bipolar Zero data  |      | 59.4  | 78    | mW   |
|                                  |                                                    | $f_S = 96\text{kHz}$ , Input is Bipolar Zero data  |      | 61.2  |       |      |
|                                  |                                                    | $f_S = 192\text{kHz}$ , Input is Bipolar Zero data |      | 64.8  |       |      |
|                                  | Power Dissipation, $DV_{DD} = 1.8\text{V}^{(6)}$   | $f_S = 48\text{kHz}$ , Input is 1kHz -1dBFS data   |      | 99    | 130.8 | mW   |
|                                  |                                                    | $f_S = 96\text{kHz}$ , Input is 1kHz -1dBFS data   |      | 100.8 |       |      |
|                                  |                                                    | $f_S = 192\text{kHz}$ , Input is 1kHz -1dBFS data  |      | 104.4 |       |      |
|                                  | Power Dissipation, $DV_{DD} = 1.8\text{V}^{(7)}$   | $f_S = \text{N/A}$ , Power Down Mode               |      | 1.2   |       | mW   |
|                                  | Power Dissipation, $DV_{DD} = 3.3\text{V}^{(5)}$   | $f_S = 48\text{kHz}$ , Input is Bipolar Zero data  |      | 79.2  | 103   | mW   |
|                                  |                                                    | $f_S = 96\text{kHz}$ , Input is Bipolar Zero data  |      | 82.5  |       |      |
|                                  |                                                    | $f_S = 192\text{kHz}$ , Input is Bipolar Zero data |      | 89.1  |       |      |
|                                  | Power Dissipation, $DV_{DD} = 3.3\text{V}^{(6)}$   | $f_S = 48\text{kHz}$ , Input is 1kHz -1dBFS data   |      | 118.8 | 155   | mW   |
|                                  |                                                    | $f_S = 96\text{kHz}$ , Input is 1kHz -1dBFS data   |      | 122.1 |       |      |
|                                  |                                                    | $f_S = 192\text{kHz}$ , Input is 1kHz -1dBFS data  |      | 128.7 |       |      |
|                                  | Power Dissipation, $DV_{DD} = 3.3\text{V}^{(7)}$   | $f_S = \text{N/A}$ , Power Down Mode               |      | 2.3   | 4.0   | mW   |

(5) Input is Bipolar Zero data.

(6) Input is 1kHz -1dBFS data

(7) Power Down Mode, with LRCK, BCK, and SCK halted at Low level.

## TYPICAL CHARACTERISTICS

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{V}$ ,  $f_S = 48\text{kHz}$ , system clock =  $512 f_S$  and 24-bit data unless otherwise noted.

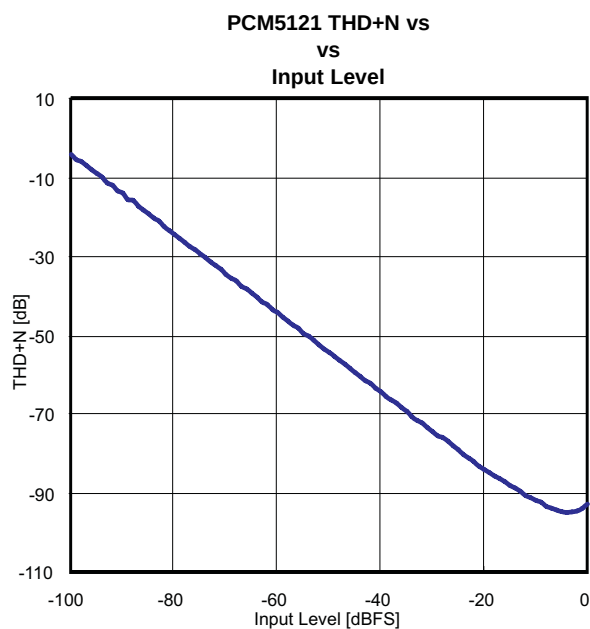


Figure 2.

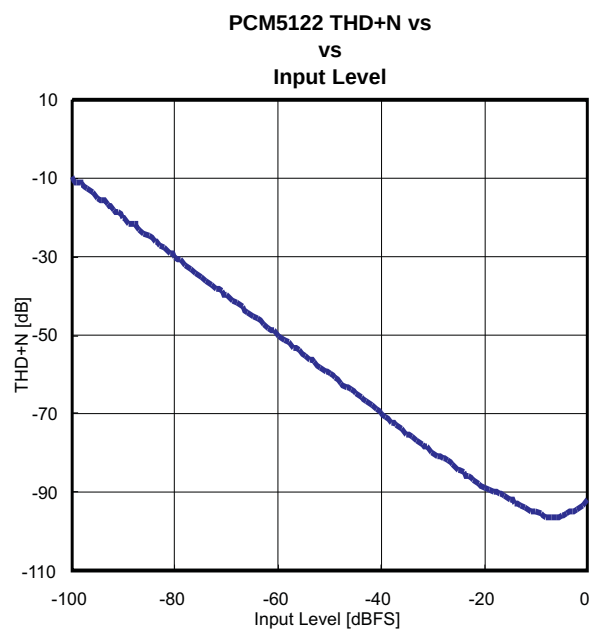


Figure 3.

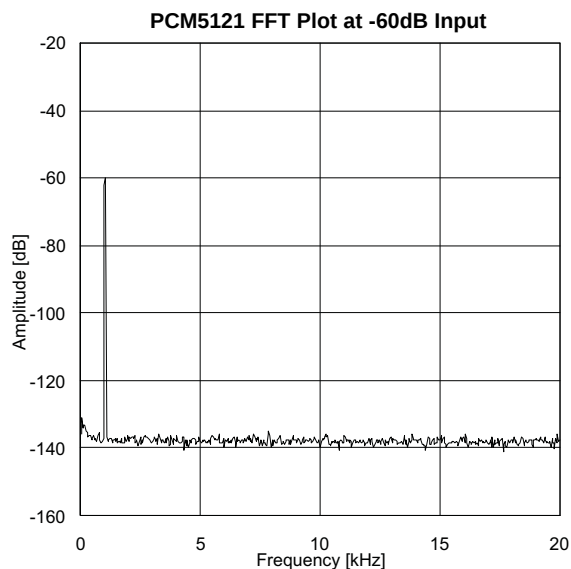


Figure 4.

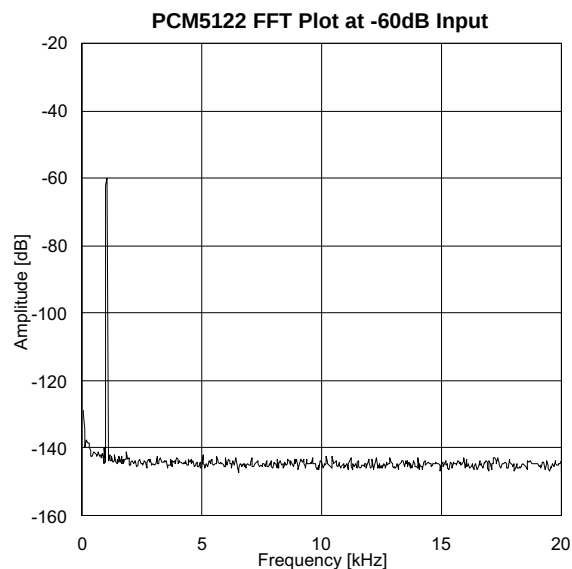


Figure 5.

### TYPICAL CHARACTERISTICS (continued)

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{V}$ ,  $f_S = 48\text{kHz}$ , system clock =  $512 f_S$  and 24-bit data unless otherwise noted.

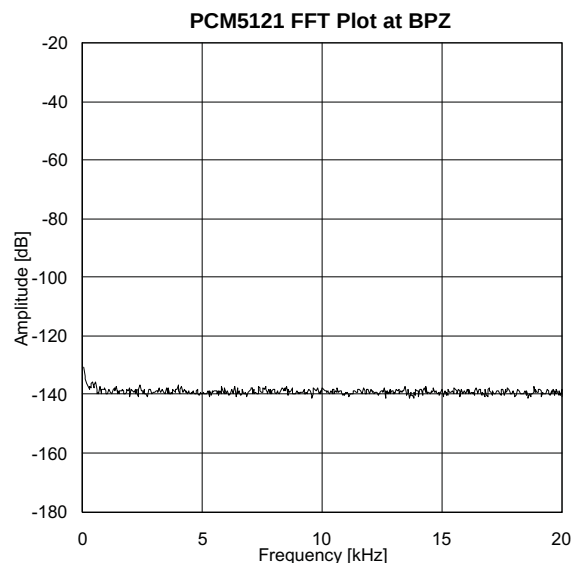


Figure 6.

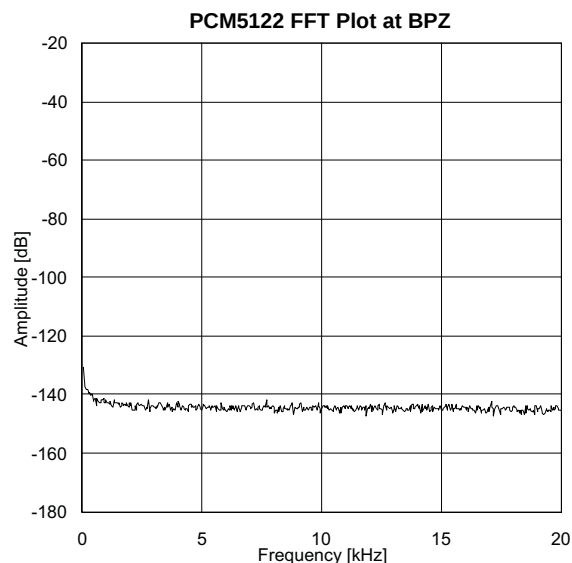


Figure 7.

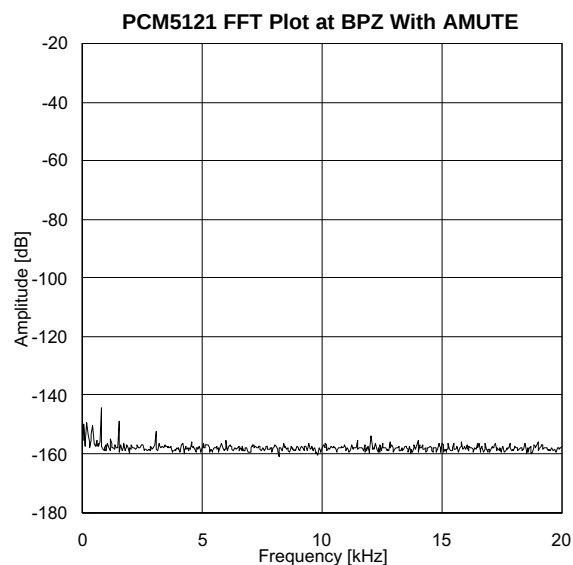


Figure 8.

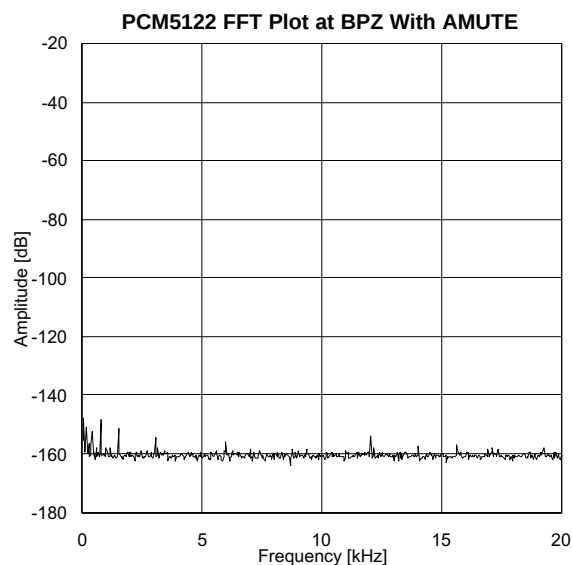


Figure 9.

## TYPICAL CHARACTERISTICS (continued)

All specifications at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{V}$ ,  $f_S = 48\text{kHz}$ , system clock =  $512 f_S$  and 24-bit data unless otherwise noted.

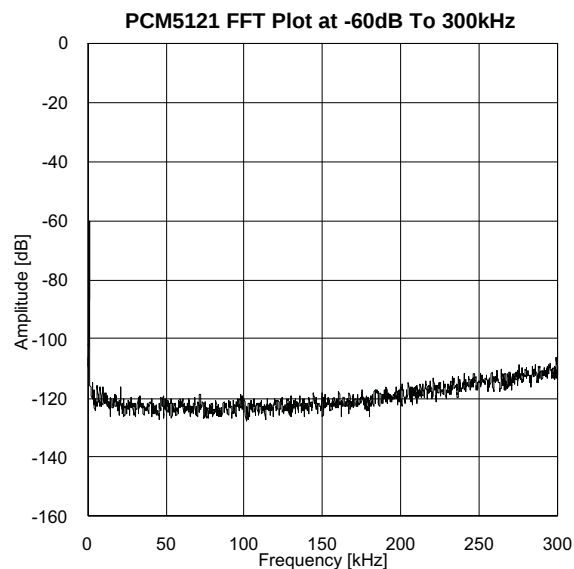


Figure 10.

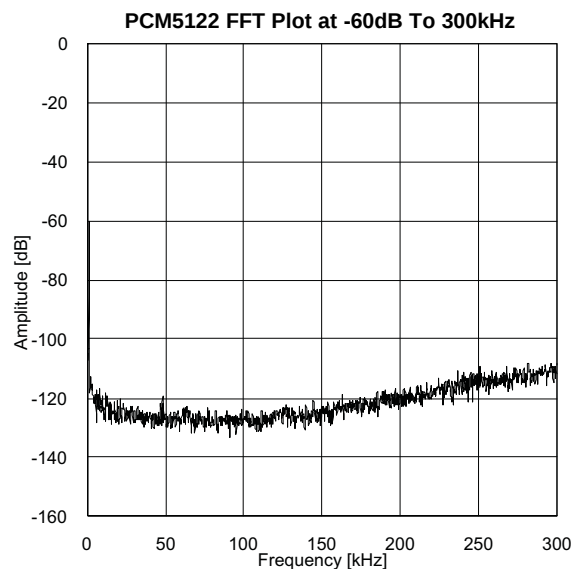


Figure 11.

## APPLICATION INFORMATION

## Typical Application Circuits

The PCM512x devices can be operated in a variety of configurations to support a wide range of applications. Figure 12 through Figure 21 show different combinations of power supplies, control methods, and VCOM/VREF usage.

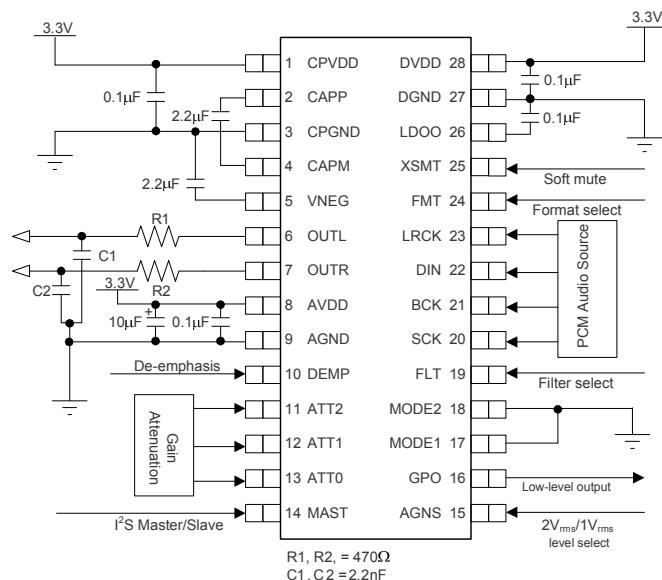


Figure 12. Hardwired Control Mode, DVDD=3.3V

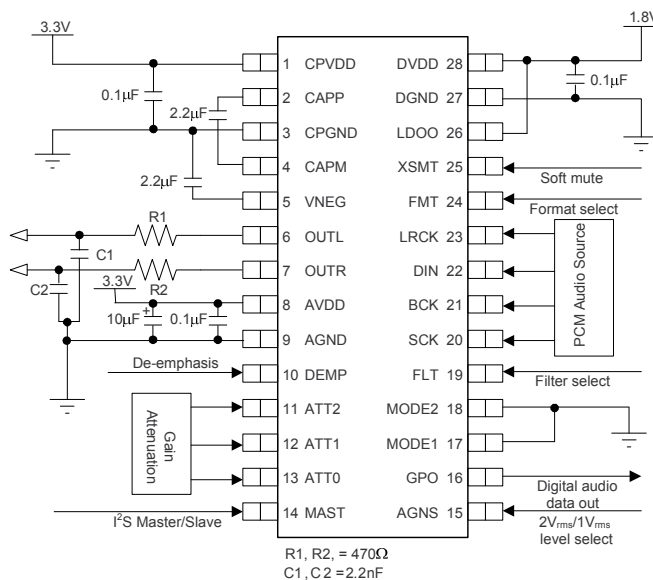


Figure 13. Hardwired Control Mode, DVDD=1.8V

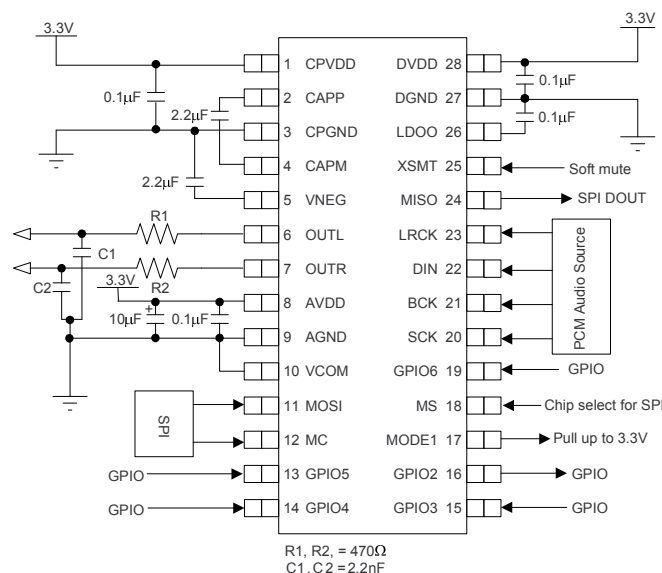


Figure 14. SPI Control, VREF Mode, DVDD=3.3V

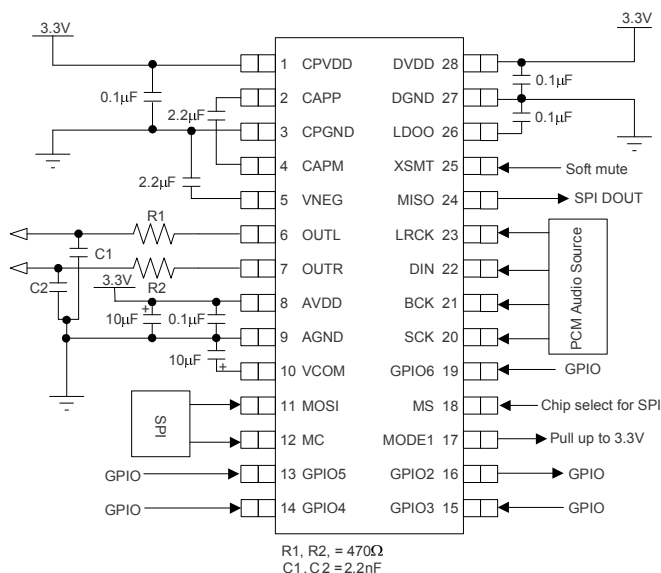
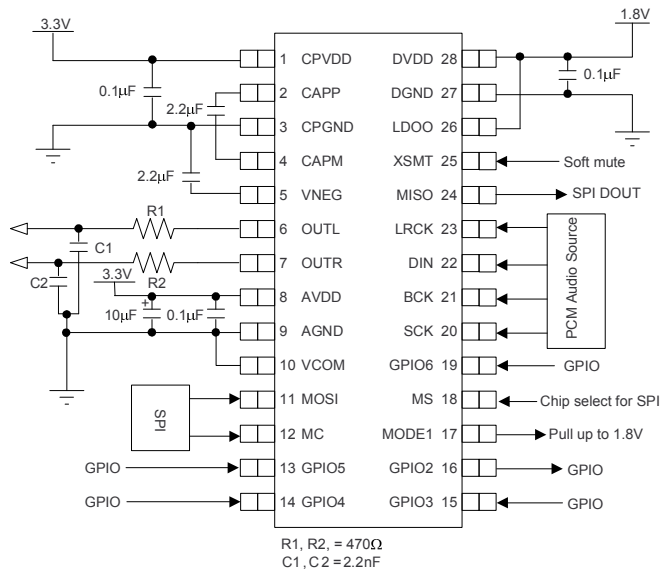
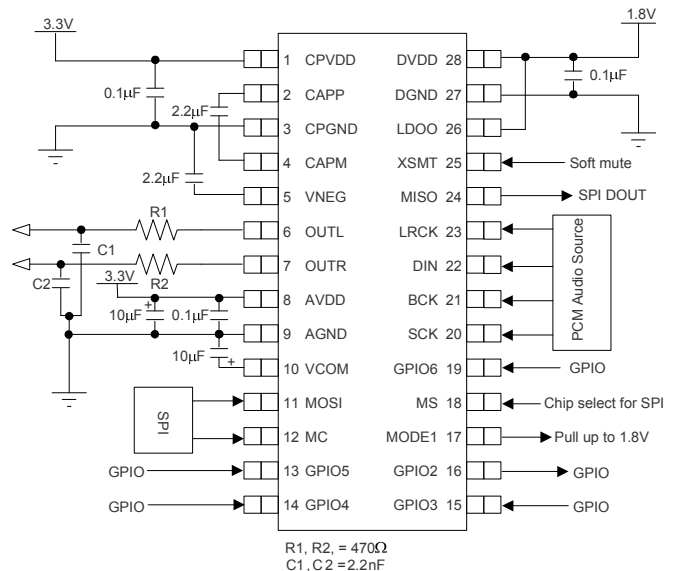


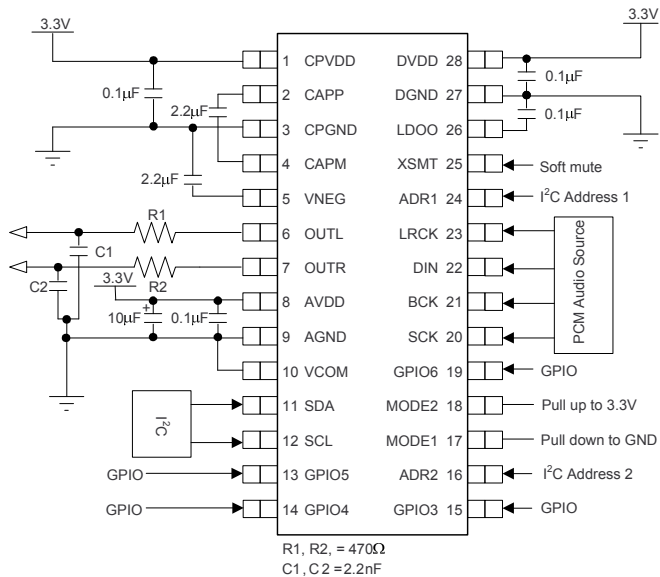
Figure 15. SPI Control, VCOM Mode, DVDD=3.3V



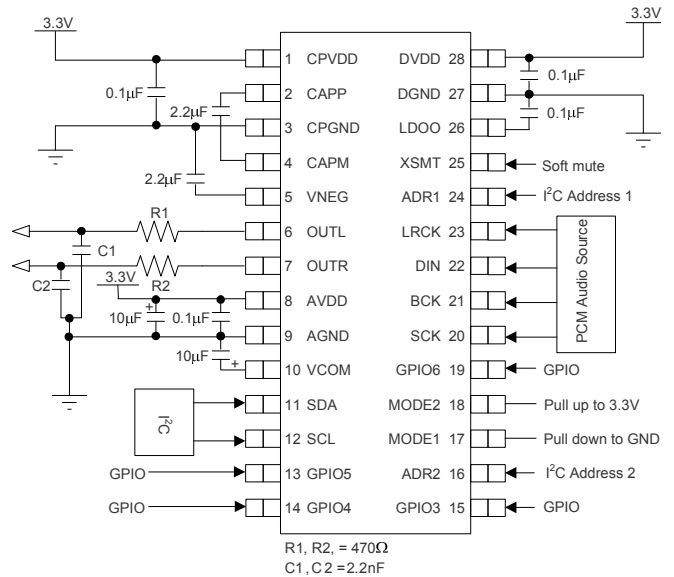
**Figure 16. SPI Control, VREF Mode, DVDD=1.8V**



**Figure 17. SPI Control, VCOM Mode, DVDD=1.8V**



**Figure 18. I²C Control, VREF Mode, DVDD=3.3V**



**Figure 19. I²C Control, VCOM Mode, DVDD=3.3V**

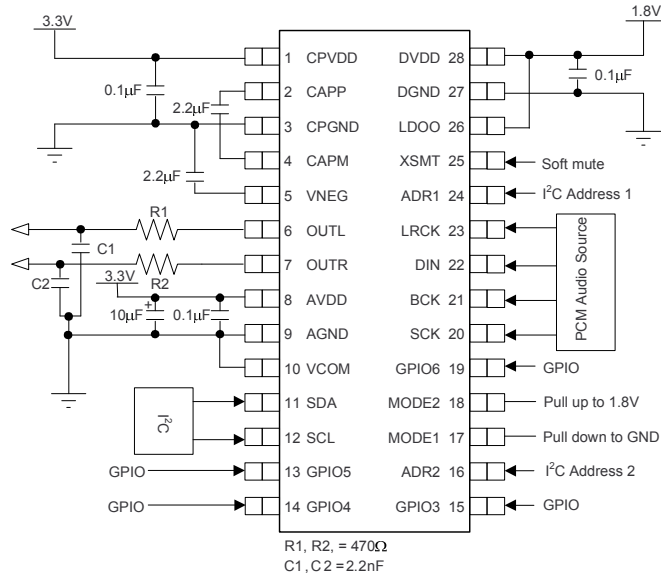


Figure 20. I²C Control, VREF Mode, DVDD=1.8V

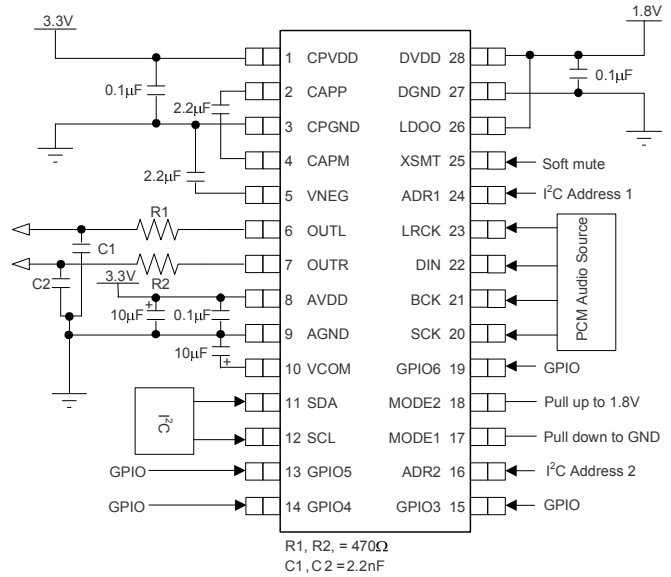


Figure 21. I²C Control, VCOM Mode, DVDD=1.8V

## Analog Outputs

The PCM512x devices include a two-channel DAC, with single-ended outputs. The full-scale output voltage is  $2.1V_{rms}$  with ground center output. A dc-coupled load is supported in addition to an ac-coupled load, if the load resistance conforms to the specification. The PCM512x DAC outputs on the OUTL and OUTR terminals have market-leading low out-of-band noise, which offer up to 20dB lower out-of-band noise compared with existing DAC technology.

Most applications require an external low-pass RC filter ( $470\Omega + 2.2nF$ ) to provide sufficient out-of-band noise rejection. This RC filter provides the added advantage of improved protection against ESD damage. Further discussion of DAC post-filter circuits is provided in the *PCM512x Application Reference Guide*, SLAU348.

## Voltage Reference and Output Levels

The PCM512x has an internal, fixed band-gap reference voltage, with default operation in VREF mode. No external decoupling capacitor is required for this mode. VREF mode provides  $2.1V_{rms}$  full-scale output at both AVDD levels.

The PCM512x can be operated with a common-mode voltage output (VCOM mode) at the VCOM pin by setting Page 1, Register 1, D(0) to 1. In this mode, an external decoupling capacitor is required.

When using this DAC in VREF mode, the output-signal voltage is independent of the power-supply voltage: The D/A conversion gain in VREF mode yields a  $2.1V_{rms}$  output voltage with a digital full-scale input. However, in VREF mode, an output waveform may clip due to the limitations that may be present in the analog power supply voltage. On the other hand, the full-scale output voltage in VCOM mode is proportional to the analog power supply AVDD. Example,  $(2.1 \times AVDD / 3.3) V_{rms}$ .

## Mode Switching Sequence, From VREF Mode to VCOM Mode

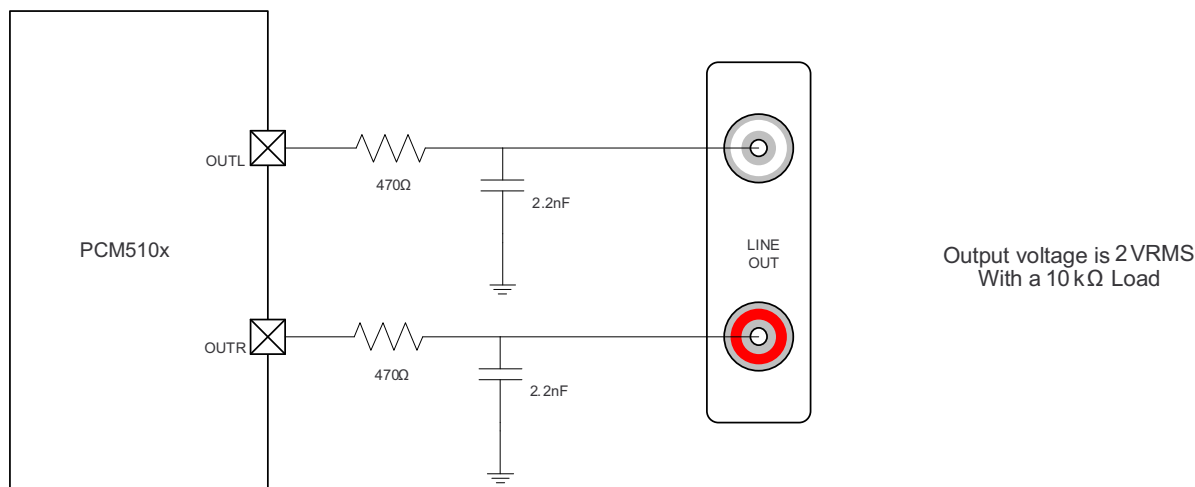
Following register setting sequence is recommended for changing VREF mode to VCOM mode.

- |                        |                                             |
|------------------------|---------------------------------------------|
| 1. Page 0 / Register 2 | RQST = 1: Standby mode                      |
| 2. Page 1 / Register 8 | RCMF = 1: Fast ramp up → on                 |
| 3. Page 1 / Register 9 | VCPD = 0: VCOM is power on                  |
| 4.                     | Wait 3ms with external capacitor = $1\mu F$ |
| 5. Page 1 / Register 8 | RCMF = 0: Fast ramp up → off                |
| 6. Page 1 / Register 1 | OSEL = 1: VCOM mode                         |
| 7. Page 0 / Register 2 | RQST = 0: Normal mode                       |

## Recommended Output Filter for the PCM512x

The diagram in [Figure 22](#) shows the recommended output filter for the PCM512x. The new PCM512x next-generation current segment architecture offers excellent out-of-band noise, making a traditional 20kHz low pass filter a thing of the past.

The RC settings below offer a -3dB filter point at 153kHz (approx), giving the DAC the ability to reproduce virtually all frequencies through to its maximum sampling rate of 384kHz.

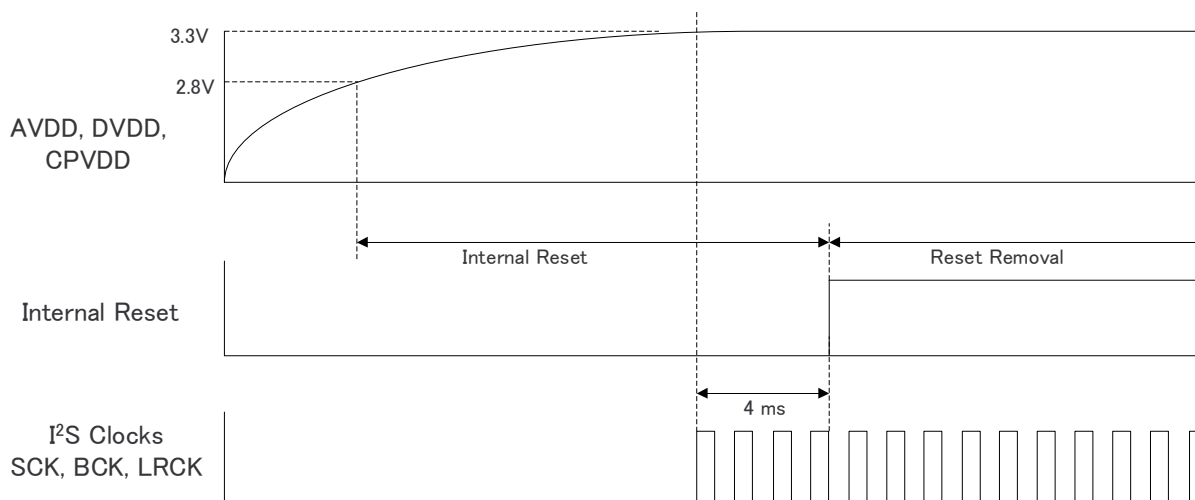


**Figure 22. Recommended Output Lowpass Filter for 10kΩ Operation**

## Reset and System Clock Functions

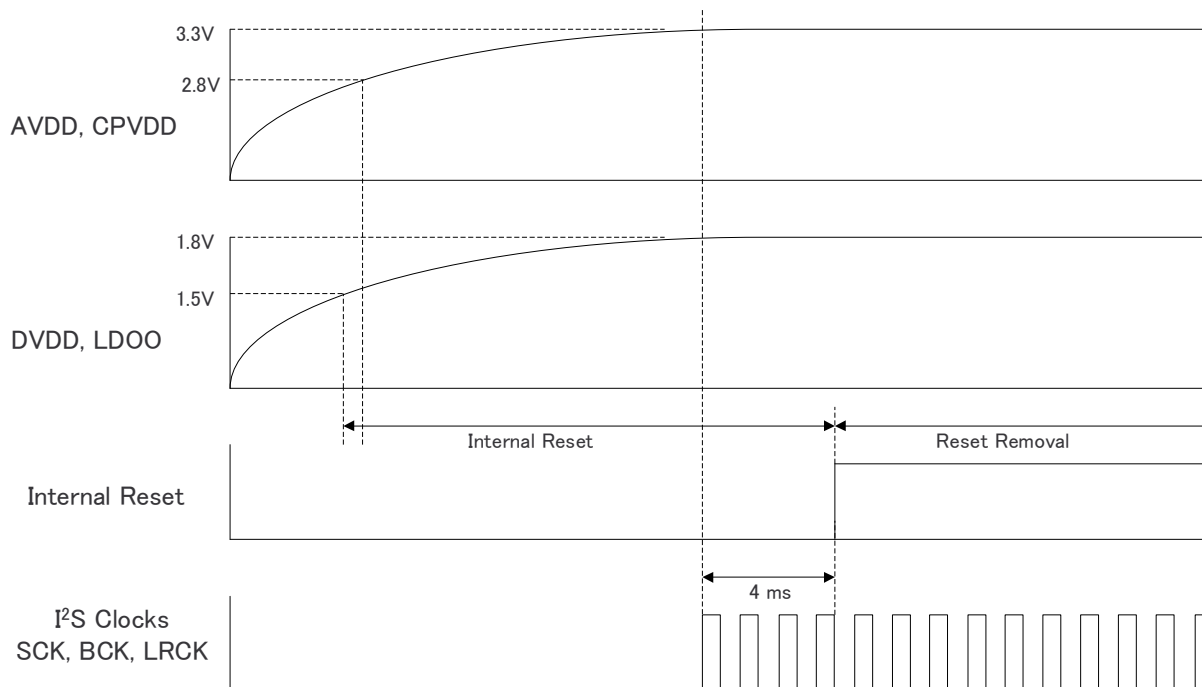
### Power-On Reset Function

The PCM512x includes a power-on reset function shown in [Figure 23](#). With  $V_{DD} > 2.8V$ , the power-on reset function is enabled. After the initialization period, the PCM512x is set to its default reset state.



**Figure 23. Power-On Reset Timing, DVDD = 3.3V**

The PCM512x includes a power-on reset function shown in [Figure 24](#) operating at DVDD=1.8V. With AVDD greater than approximately 2.8V, and PVDD greater than approximately 2.8V, and DVDD greater than approximately 1.5V, the power-on reset function is enabled. After the initialization period, the PCM512x is set to its default reset state.



**Figure 24. Power-On Reset Timing, DVDD = 1.8V**

## System Clock Input

The PCM512x requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 20) and supports up to 50MHz. The PCM512x system-clock detection circuit automatically senses the system-clock frequency. Common audio sampling frequencies of 8kHz, 16kHz, 32kHz - 44.1kHz - 48kHz, 88.2kHz - 96kHz, 176.4kHz - 192kHz, and 384kHz with  $\pm 4\%$  tolerance are supported. The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge Pump (NCP) automatically. Table 6 shows examples of system clock frequencies for common audio sampling rates.

SCK rates that are not common to standard audio clocks, between 1MHz and 50MHz, are only supported in software mode by configuring various PLL and clock-divider registers. This programmability allows the device to become a clock master and drive the host serial port with LRCK and BCK, from a non-audio related clock (for example, using 12MHz to generate 44.1kHz (LRCK) and 2.8224MHz (BCK) ).

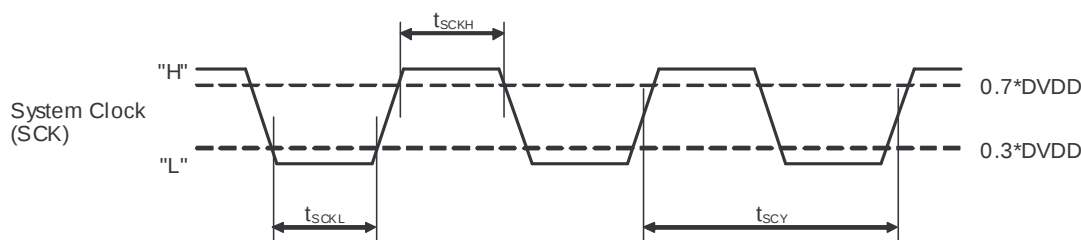
Figure 25 shows the timing requirements for the system clock input. For optimal performance, use a clock source with low phase jitter and noise.

**Table 6. System Master Clock Inputs for Audio Related Clocks**

| Sampling Frequency | System Clock Frequency ( $f_{SCK}$ ) (MHz) |                        |                       |                  |                  |                  |                  |                  |                  |                  |                  |                  |
|--------------------|--------------------------------------------|------------------------|-----------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
|                    | 64 $f_s$                                   | 128 $f_s$              | 192 $f_s$             | 256 $f_s$        | 384 $f_s$        | 512 $f_s$        | 768 $f_s$        | 1024 $f_s$       | 1152 $f_s$       | 1536 $f_s$       | 2048 $f_s$       | 3072 $f_s$       |
| 8 kHz              | — <sup>(1)</sup>                           | 1.0240 <sup>(2)</sup>  | 1.5360 <sup>(2)</sup> | 2.0480           | 3.0720           | 4.0960           | 6.1440           | 8.1920           | 9.2160           | 12.2880          | 16.3840          | 24.5760          |
| 16 kHz             | — <sup>(1)</sup>                           | 2.0480 <sup>(2)</sup>  | 3.0720 <sup>(2)</sup> | 4.0960           | 6.1440           | 8.1920           | 12.2880          | 16.3840          | 18.4320          | 24.5760          | 36.8640          | 49.1520          |
| 32 kHz             | — <sup>(1)</sup>                           | 4.0960 <sup>(2)</sup>  | 6.1440 <sup>(2)</sup> | 8.1920           | 12.2880          | 16.3840          | 24.5760          | 32.7680          | 36.8640          | 49.1520          | — <sup>(1)</sup> | — <sup>(1)</sup> |
| 44.1 kHz           | — <sup>(1)</sup>                           | 5.6488 <sup>(2)</sup>  | 8.4672 <sup>(2)</sup> | 11.2896          | 16.9344          | 22.5792          | 33.8688          | 45.1584          | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> |
| 48 kHz             | — <sup>(1)</sup>                           | 6.1440 <sup>(2)</sup>  | 9.2160 <sup>(2)</sup> | 12.2880          | 18.4320          | 24.5760          | 36.8640          | 49.1520          | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> |
| 88.2 kHz           | — <sup>(1)</sup>                           | 11.2896 <sup>(2)</sup> | 16.9344               | 22.5792          | 33.8688          | 45.1584          | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> |
| 96 kHz             | — <sup>(1)</sup>                           | 12.2880 <sup>(2)</sup> | 18.4320               | 24.5760          | 36.8640          | 49.1520          | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> |
| 176.4 kHz          | — <sup>(1)</sup>                           | 22.5792                | 33.8688               | 45.1584          | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> |
| 192 kHz            | — <sup>(1)</sup>                           | 24.5760                | 36.8640               | 49.1520          | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> |
| 384 kHz            | 24.5760                                    | 49.1520                | — <sup>(1)</sup>      | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> | — <sup>(1)</sup> |

(1) This system clock rate is not supported for the given sampling frequency.

(2) This system clock rate is supported by PLL mode.



**Figure 25. Timing Requirements for SCK Input**

**Table 7. Timing Requirements for SCK Input**

|            | Parameters                     | Min       | Max  | Unit |
|------------|--------------------------------|-----------|------|------|
| $t_{SCY}$  | System clock pulse cycle time  | 20        | 1000 | ns   |
| $t_{SCKH}$ | System clock pulse width, High | DVDD=1.8V | 8    | ns   |
|            |                                | DVDD=3.3V | 9    |      |
| $t_{SCKL}$ | System clock pulse width, Low  | DVDD=1.8V | 8    | ns   |
|            |                                | DVDD=3.3V | 9    |      |

## System Clock PLL Mode

The system clock PLL mode allows designers to use a simple 3-wire I<sup>2</sup>S audio source when driving the DAC. The 3-wire source reduces the need for a high frequency SCK, making PCB layout easier, and reduces high frequency electromagnetic interference.

The device starts up expecting an external SCK input, but if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, then the internal PLL starts, automatically generating an internal SCK from the BCK reference. The PCM512x disables the internal PLL when an external SCK is supplied; specific BCK rates are required to generate an appropriate master clock. [Table 8](#) describes the minimum and maximum BCK per LRCK for the integrated PLL to automatically generate an internal SCK.

In hardwired mode, the internal PLL is disabled as soon as an external SCK is supplied; specific BCK rates are required to generate an appropriate master clock. [Table 8](#) lists the minimum and maximum BCK per LRCK for the Integrated PLL to automatically generate an internal SCK.

In software mode, the user must set all the PLL registers and clock divider registers for referencing BCK. See [Clock Generation and PLL](#) for more information.

**Table 8. BCK Rates (MHz) by LRCK Sample Rate for PCM512x PLL Operation**

| Sample f (kHz) | BCK (f <sub>S</sub> ) |        |
|----------------|-----------------------|--------|
|                | 32                    | 64     |
| 8              | -                     | -      |
| 16             | -                     | 1.024  |
| 32             | 1.024                 | 2.048  |
| 44.1           | 1.4112                | 2.8224 |
| 48             | 1.536                 | 3.072  |
| 96             | 3.072                 | 6.144  |
| 192            | 6.144                 | 12.288 |
| 384            | 12.288                | 24.576 |

## Clock Generation and PLL

The PCM512x supports a wide range of options to generate the required clocks for the DAC section as well as interface and other control blocks as shown in [Figure 26](#).

The clocks for the PLL require a source reference clock. This clock is sourced as the incoming BCK or SCK.

The source reference clock for the PLL reference clock is selected by programming the SRCREF value on Page 0, Register 13, D(6:4). The PLL reference clock can then be routed through highly-flexible clock dividers shown in [Figure 26](#) to generate the various clocks required for the DAC, Negative Charge Pump (NCP), Internal modulator and audio processor sections. The PCM512x provides several programmable clock dividers to achieve a variety of sampling rates for the DAC and clocks for the NCP, OSR, and the audio processor. OSRCK for OSR must be set at 16f<sub>S</sub> frequency by DOSR on Page0, Register 30, D(6:0).

If PLL functionality isn't required, set the PLEN value on Page 0, Register 4, D(0) to 0. In this situation, an external SCK is required.

**Table 9. PLL Configuration Registers**

| Clock multiplexer | Function                      | Bits                        |
|-------------------|-------------------------------|-----------------------------|
| SRCREF            | PLL Reference                 | Page 0, Register 13, D(6:4) |
| Divider           | Function                      | Bits                        |
| DDSP              | audio processor clock divider | Page 0, Register 27, D(6:0) |
| DDAC              | DAC clock divider             | Page 0, Register 28, D(6:0) |
| DNCP              | NCP clock divider             | Page 0, Register 29, D(6:0) |
| DOSR              | OSR clock divider             | Page 0, Register 30, D(6:0) |
| DBCK              | External BCK Div              | Page 0, Register 32, D(6:0) |

Table 9. PLL Configuration Registers (continued)

|      |                   |                             |
|------|-------------------|-----------------------------|
| DLRK | External LRCK Div | Page 0, Register 33, D(7:0) |
|------|-------------------|-----------------------------|

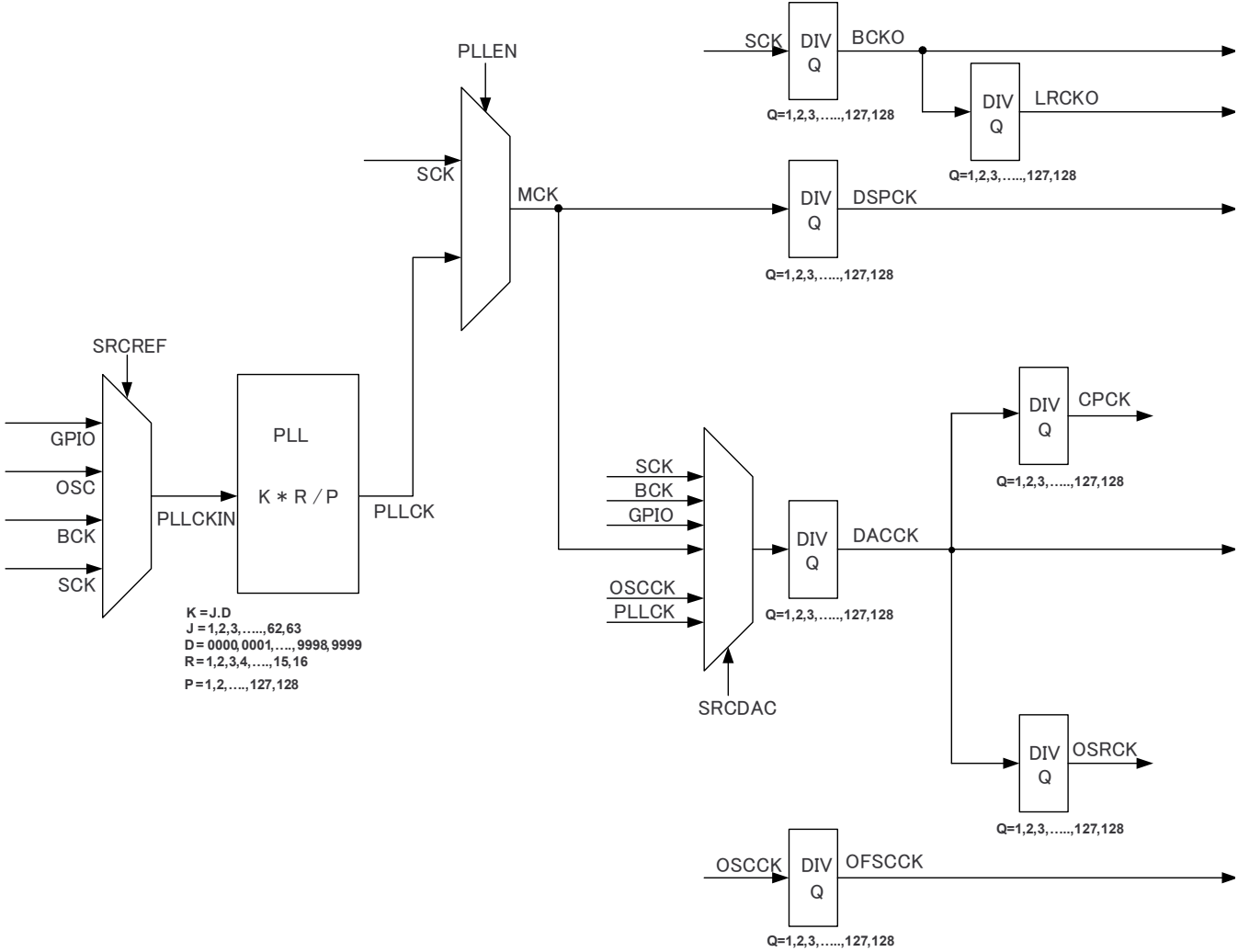


Figure 26. PLL Clock Source and Clock Distribution

## PLL Calculation

The PCM512x has an on-chip PLL with fractional multiplication to generate the clock frequency needed by the audio DAC, Negative Charge Pump, Modulator and Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL input (PLLCKIN) supports clock frequencies from 512kHz to 50MHz and is register programmable to enable generation of required sampling rates with fine precision.

The PLL is enabled by default. The PLL can be turned on by writing to Page 0, Register 4, D(0). When the PLL is enabled, the PLL output clock PLLCK is given by [Equation 1](#):

$$\text{PLLCK} = \frac{\text{PLLCKIN} \times R \times J.D}{P} \quad \text{or} \quad \text{PLLCK} = \frac{\text{PLLCKIN} \times R \times K}{P} \quad (1)$$

R = 1, 2, 3, 4, ... , 15, 16

J = 4, 5, 6, ... 63, and D = 0000, 0001, 0002, ... 9999

K = [J value].[D value]

P = 1, 2, 3, ... 15

R, J, D, and P are programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

### Examples:

- If K = 8.5, then J = 8, D = 5000
- If K = 7.12, then J = 7, D = 1200
- If K = 14.03, then J = 14, D = 0300
- If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, the following conditions must be satisfied:

- $1\text{MHz} \leq (\text{PLLCKIN} / P) \leq 20\text{MHz}$
- $64\text{MHz} \leq (\text{PLLCKIN} \times K \times R / P) \leq 100\text{MHz}$  (in VREF mode)
- $72\text{MHz} \leq (\text{PLLCKIN} \times K \times R / P) \leq 86\text{MHz}$  (in VCOM mode)
- $1 \leq J \leq 63$

When the PLL is enabled and D ≠ 0000, the following conditions must be satisfied:

- $6.667\text{MHz} \leq \text{PLLCKIN} / P \leq 20\text{MHz}$
- $64\text{MHz} \leq (\text{PLLCKIN} \times K \times R / P) \leq 100\text{MHz}$  (in VREF mode)
- $72\text{MHz} \leq (\text{PLLCKIN} \times K \times R / P) \leq 86\text{MHz}$  (in VCOM mode)
- $4 \leq J \leq 11$
- R = 1

When the PLL is enabled,

- $f_s = (\text{PLLCKIN} \times K \times R) / (2048 \times P)$
- The value of N is selected so that  $f_s \times N = \text{PLLCKIN} \times K \times R / P$  is in the allowable range.

**Example:** MCLK = 12MHz and  $f_s = 44.1\text{kHz}$ , (N=2048)

Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

**Example:** MCLK = 12MHz and  $f_s = 48.0\text{kHz}$ , (N=2048)

Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

Values are written to the registers in [Table 10](#).

**Table 10. PLL Registers**

| Divider | Function   | Bits                        |
|---------|------------|-----------------------------|
| PLLE    | PLL enable | Page 0, Register 4, D(0)    |
| PPDV    | PLL P      | Page 0, Register 20, D(3:0) |
| PJDV    | PLL J      | Page 0, Register 21, D(5:0) |
| PDDV    | PLL D      | Page 0, Register 22, D(5:0) |
|         |            | Page 0, Register 23, D(7:0) |
| PRDV    | PLL R      | Page 0, Register 24, D(3:0) |

**Table 11. PLL Configuration Recommendations**

| Column        | Description                                                                                                                                                                                                                                                                                                                                   |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $f_s$ (kHz)   | Sampling frequency                                                                                                                                                                                                                                                                                                                            |
| RSCK          | Ratio between sampling frequency and SCK frequency (SCK frequency = RSCK x sampling frequency)                                                                                                                                                                                                                                                |
| SCK (MHz)     | System master clock frequency at SCK input (pin 20)                                                                                                                                                                                                                                                                                           |
| PLL VCO (MHz) | PLL VCO frequency as PLLCK in <a href="#">Figure 26</a>                                                                                                                                                                                                                                                                                       |
| P             | One of the PLL coefficients in <a href="#">Equation 1</a>                                                                                                                                                                                                                                                                                     |
| PLL REF (MHz) | Internal reference clock frequency which is produced by SCK / P                                                                                                                                                                                                                                                                               |
| $M = K * R$   | The final PLL multiplication factor computed from K and R as described in <a href="#">Equation 1</a>                                                                                                                                                                                                                                          |
| $K = J.D$     | One of the PLL coefficients in <a href="#">Equation 1</a>                                                                                                                                                                                                                                                                                     |
| R             | One of the PLL coefficients in <a href="#">Equation 1</a>                                                                                                                                                                                                                                                                                     |
| PLL $f_s$     | Ratio between $f_s$ and PLL VCO frequency (PLL VCO / $f_s$ )                                                                                                                                                                                                                                                                                  |
| DSP $f_s$     | Ratio between audio processor operating clock rate and $f_s$ (PLL $f_s$ / NMAC)                                                                                                                                                                                                                                                               |
| NMAC          | The audio processor clock divider value in <a href="#">Table 9</a>                                                                                                                                                                                                                                                                            |
| DSP CLK (MHz) | The audio processor operating frequency as DSPCK in <a href="#">Figure 26</a>                                                                                                                                                                                                                                                                 |
| MOD $f_s$     | Ratio between DAC operating clock frequency and $f_s$ (PLL $f_s$ / NDAC)                                                                                                                                                                                                                                                                      |
| MOD f (kHz)   | DAC operating frequency as DACCK in <a href="#">Figure 26</a>                                                                                                                                                                                                                                                                                 |
| NDAC          | DAC clock divider value in <a href="#">Table 9</a>                                                                                                                                                                                                                                                                                            |
| DOSR          | OSR clock divider value in <a href="#">Table 9</a> for generating OSRCK in <a href="#">Figure 26</a> . DOSR must be chosen so that MOD $f_s$ / DOSR = 16 for correct operation.                                                                                                                                                               |
| NCP           | NCP (negative charge pump) clock divider value in <a href="#">Table 9</a>                                                                                                                                                                                                                                                                     |
| CP f          | Negative charge pump clock frequency ( $f_s * \text{MOD } f_s / \text{NCP}$ )                                                                                                                                                                                                                                                                 |
| % Error       | <p>Percentage of error between PLL VCO / PLL <math>f_s</math> and <math>f_s</math> (mismatch error).</p> <ul style="list-style-type: none"> <li>This number is typically zero but can be non-zero especially when K is not an integer (D is not zero).</li> <li>This number may be non-zero only when the PCM512xacts as a master.</li> </ul> |

**Table 12. Recommended Clock Divider Settings for PLL as Master Clock (VREF Mode)**

| f <sub>s</sub> (kHz) | RSCK | SCK (MHz) | PLL VCO (MHz) | P | PLL REF (MHz) | M = K*R | K = J.D | R | PLL f <sub>s</sub> | DSP f <sub>s</sub> | NMAC | DSP CLK (MHz) | MOD f <sub>s</sub> | MOD f (kHz) | NDAC | DOSR | % Error | NCP | CP f (kHz) |
|----------------------|------|-----------|---------------|---|---------------|---------|---------|---|--------------------|--------------------|------|---------------|--------------------|-------------|------|------|---------|-----|------------|
| 8                    | 128  | 1.024     | 98.304        | 1 | 1.024         | 96      | 48      | 2 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 8                    | 192  | 1.536     | 98.304        | 1 | 1.536         | 64      | 32      | 2 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 8                    | 256  | 2.048     | 98.304        | 1 | 2.048         | 48      | 48      | 1 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 8                    | 384  | 3.072     | 98.304        | 3 | 1.024         | 96      | 48      | 2 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 8                    | 512  | 4.096     | 98.304        | 3 | 1.365         | 72      | 36      | 2 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 8                    | 768  | 6.144     | 98.304        | 3 | 2.048         | 48      | 48      | 1 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 8                    | 1024 | 8.192     | 98.304        | 3 | 2.731         | 36      | 36      | 1 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 8                    | 1152 | 9.216     | 98.304        | 9 | 1.024         | 96      | 48      | 2 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 8                    | 1536 | 12.288    | 98.304        | 9 | 1.365         | 72      | 36      | 2 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 8                    | 2048 | 16.384    | 98.304        | 9 | 1.82          | 54      | 54      | 1 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 8                    | 3072 | 24.576    | 98.304        | 9 | 2.731         | 36      | 36      | 1 | 12288              | 1024               | 12   | 8.192         | 768                | 6144        | 16   | 48   | 0       | 4   | 1536       |
| 11.025               | 128  | 1.4112    | 90.3168       | 1 | 1.411         | 64      | 32      | 2 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 192  | 2.1168    | 90.3168       | 3 | 0.706         | 128     | 32      | 4 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 256  | 2.8224    | 90.3168       | 1 | 2.822         | 32      | 32      | 1 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 384  | 4.2336    | 90.3168       | 3 | 1.411         | 64      | 32      | 2 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 512  | 5.6448    | 90.3168       | 3 | 1.882         | 48      | 48      | 1 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 768  | 8.4672    | 90.3168       | 3 | 2.822         | 32      | 32      | 1 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 1024 | 11.2896   | 90.3168       | 3 | 3.763         | 24      | 24      | 1 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 1152 | 12.7008   | 90.3168       | 9 | 1.411         | 64      | 32      | 2 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 1536 | 16.9344   | 90.3168       | 9 | 1.882         | 48      | 48      | 1 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 2048 | 22.5792   | 90.3168       | 9 | 2.509         | 36      | 36      | 1 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 3072 | 33.8688   | 90.3168       | 9 | 3.763         | 24      | 24      | 1 | 8192               | 1024               | 8    | 11.2896       | 512                | 5644.8      | 16   | 32   | 0       | 4   | 1411.2     |
| 16                   | 64   | 1.024     | 98.304        | 1 | 1.024         | 96      | 48      | 2 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 128  | 2.048     | 98.304        | 1 | 2.048         | 48      | 48      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 192  | 3.072     | 98.304        | 1 | 3.072         | 32      | 32      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 256  | 4.096     | 98.304        | 1 | 4.096         | 24      | 24      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 384  | 6.144     | 98.304        | 3 | 2.048         | 48      | 48      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 512  | 8.192     | 98.304        | 3 | 2.731         | 36      | 36      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 768  | 12.288    | 98.304        | 3 | 4.096         | 24      | 24      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 1024 | 16.384    | 98.304        | 3 | 5.461         | 18      | 18      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 1152 | 18.432    | 98.304        | 3 | 6.144         | 16      | 16      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 1536 | 24.576    | 98.304        | 9 | 2.731         | 36      | 36      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 2048 | 32.768    | 98.304        | 9 | 3.641         | 27      | 27      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 16                   | 3072 | 49.152    | 98.304        | 9 | 5.461         | 18      | 18      | 1 | 6144               | 1024               | 6    | 16.384        | 384                | 6144        | 16   | 24   | 0       | 4   | 1536       |
| 22.05                | 64   | 1.4112    | 90.3168       | 1 | 1.411         | 64      | 32      | 2 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 128  | 2.8224    | 90.3168       | 1 | 2.822         | 32      | 32      | 1 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 192  | 4.2336    | 90.3168       | 3 | 1.411         | 64      | 32      | 2 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 256  | 5.6448    | 90.3168       | 1 | 5.645         | 16      | 16      | 1 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |

**Table 12. Recommended Clock Divider Settings for PLL as Master Clock (VREF Mode) (continued)**

| f <sub>s</sub> (kHz) | RSCK | SCK (MHz) | PLL VCO (MHz) | P | PLL REF (MHz) | M = K*R | K = J.D | R | PLL f <sub>s</sub> | DSP f <sub>s</sub> | NMAC | DSP CLK (MHz) | MOD f <sub>s</sub> | MOD f (kHz) | NDAC | DOSR | % Error | NCP | CP f (kHz) |
|----------------------|------|-----------|---------------|---|---------------|---------|---------|---|--------------------|--------------------|------|---------------|--------------------|-------------|------|------|---------|-----|------------|
| 22.05                | 384  | 8.4672    | 90.3168       | 3 | 2.822         | 32      | 32      | 1 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 512  | 11.2896   | 90.3168       | 3 | 3.763         | 24      | 24      | 1 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 768  | 16.9344   | 90.3168       | 3 | 5.645         | 16      | 16      | 1 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 1024 | 22.5792   | 90.3168       | 3 | 7.526         | 12      | 12      | 1 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 1152 | 25.4016   | 90.3168       | 9 | 2.822         | 32      | 32      | 1 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 1536 | 33.8688   | 90.3168       | 9 | 3.763         | 24      | 24      | 1 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 2048 | 45.1584   | 90.3168       | 9 | 5.018         | 18      | 18      | 1 | 4096               | 1024               | 4    | 22.5792       | 256                | 5644.8      | 16   | 16   | 0       | 4   | 1411.2     |
| 32                   | 32   | 1.024     | 98.304        | 1 | 1.024         | 96      | 48      | 2 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 48   | 1.536     | 98.304        | 1 | 1.536         | 64      | 16      | 4 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 64   | 2.048     | 98.304        | 1 | 2.048         | 48      | 24      | 2 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 128  | 4.096     | 98.304        | 1 | 4.096         | 24      | 24      | 1 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 192  | 6.144     | 98.304        | 3 | 2.048         | 48      | 48      | 1 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 256  | 8.192     | 98.304        | 2 | 4.096         | 24      | 24      | 1 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 384  | 12.288    | 98.304        | 3 | 4.096         | 24      | 24      | 1 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 512  | 16.384    | 98.304        | 3 | 5.461         | 18      | 18      | 1 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 768  | 24.576    | 98.304        | 3 | 8.192         | 12      | 12      | 1 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 1024 | 32.768    | 98.304        | 3 | 10.923        | 9       | 9       | 1 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 1152 | 36.864    | 98.304        | 9 | 4.096         | 24      | 24      | 1 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 32                   | 1536 | 49.152    | 98.304        | 6 | 8.192         | 12      | 12      | 1 | 3072               | 1024               | 3    | 32.768        | 192                | 6144        | 16   | 12   | 0       | 4   | 1536       |
| 44.1                 | 32   | 1.4112    | 90.3168       | 1 | 1.411         | 64      | 32      | 2 | 2048               | 1024               | 2    | 45.1584       | 128                | 5644.8      | 16   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 64   | 2.8224    | 90.3168       | 1 | 2.822         | 32      | 16      | 2 | 2048               | 1024               | 2    | 45.1584       | 128                | 5644.8      | 16   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 128  | 5.6448    | 90.3168       | 1 | 5.645         | 16      | 16      | 1 | 2048               | 1024               | 2    | 45.1584       | 128                | 5644.8      | 16   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 192  | 8.4672    | 90.3168       | 3 | 2.822         | 32      | 32      | 1 | 2048               | 1024               | 2    | 45.1584       | 128                | 5644.8      | 16   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 256  | 11.2896   | 90.3168       | 2 | 5.645         | 16      | 16      | 1 | 2048               | 1024               | 2    | 45.1584       | 128                | 5644.8      | 16   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 384  | 16.9344   | 90.3168       | 3 | 5.645         | 16      | 16      | 1 | 2048               | 1024               | 2    | 45.1584       | 128                | 5644.8      | 16   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 512  | 22.5792   | 90.3168       | 3 | 7.526         | 12      | 12      | 1 | 2048               | 1024               | 2    | 45.1584       | 128                | 5644.8      | 16   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 768  | 33.8688   | 90.3168       | 3 | 11.29         | 8       | 8       | 1 | 2048               | 1024               | 2    | 45.1584       | 128                | 5644.8      | 16   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 1024 | 45.1584   | 90.3168       | 3 | 15.053        | 6       | 6       | 1 | 2048               | 1024               | 2    | 45.1584       | 128                | 5644.8      | 16   | 8    | 0       | 4   | 1411.2     |
| 48                   | 32   | 1.536     | 98.304        | 1 | 1.536         | 64      | 32      | 2 | 2048               | 1024               | 2    | 49.152        | 128                | 6144        | 16   | 8    | 0       | 4   | 1536       |
| 48                   | 64   | 3.072     | 98.304        | 1 | 3.072         | 32      | 16      | 2 | 2048               | 1024               | 2    | 49.152        | 128                | 6144        | 16   | 8    | 0       | 4   | 1536       |
| 48                   | 128  | 6.144     | 98.304        | 1 | 6.144         | 16      | 16      | 1 | 2048               | 1024               | 2    | 49.152        | 128                | 6144        | 16   | 8    | 0       | 4   | 1536       |
| 48                   | 192  | 9.216     | 98.304        | 3 | 3.072         | 32      | 32      | 1 | 2048               | 1024               | 2    | 49.152        | 128                | 6144        | 16   | 8    | 0       | 4   | 1536       |
| 48                   | 256  | 12.288    | 98.304        | 2 | 6.144         | 16      | 16      | 1 | 2048               | 1024               | 2    | 49.152        | 128                | 6144        | 16   | 8    | 0       | 4   | 1536       |
| 48                   | 384  | 18.432    | 98.304        | 3 | 6.144         | 16      | 16      | 1 | 2048               | 1024               | 2    | 49.152        | 128                | 6144        | 16   | 8    | 0       | 4   | 1536       |
| 48                   | 512  | 24.576    | 98.304        | 3 | 8.192         | 12      | 12      | 1 | 2048               | 1024               | 2    | 49.152        | 128                | 6144        | 16   | 8    | 0       | 4   | 1536       |
| 48                   | 768  | 36.864    | 98.304        | 3 | 12.288        | 8       | 8       | 1 | 2048               | 1024               | 2    | 49.152        | 128                | 6144        | 16   | 8    | 0       | 4   | 1536       |
| 48                   | 1024 | 49.152    | 98.304        | 3 | 16.384        | 6       | 6       | 1 | 2048               | 1024               | 2    | 49.152        | 128                | 6144        | 16   | 8    | 0       | 4   | 1536       |
| 96                   | 32   | 3.072     | 98.304        | 1 | 3.072         | 32      | 16      | 2 | 1024               | 512                | 2    | 49.152        | 64                 | 6144        | 16   | 4    | 0       | 4   | 1536       |

**Table 12. Recommended Clock Divider Settings for PLL as Master Clock (VREF Mode) (continued)**

| f <sub>s</sub> (kHz) | RSCK | SCK (MHz) | PLL VCO (MHz) | P | PLL REF (MHz) | M = K*R | K = J.D | R | PLL f <sub>s</sub> | DSP f <sub>s</sub> | NMAC | DSP CLK (MHz) | MOD f <sub>s</sub> | MOD f (kHz) | NDAC | DOSR | % Error | NCP | CP f (kHz) |
|----------------------|------|-----------|---------------|---|---------------|---------|---------|---|--------------------|--------------------|------|---------------|--------------------|-------------|------|------|---------|-----|------------|
| 96                   | 48   | 4.608     | 98.304        | 3 | 1.536         | 64      | 32      | 2 | 1024               | 512                | 2    | 49.152        | 64                 | 6144        | 16   | 4    | 0       | 4   | 1536       |
| 96                   | 64   | 6.144     | 98.304        | 1 | 6.144         | 16      | 8       | 2 | 1024               | 512                | 2    | 49.152        | 64                 | 6144        | 16   | 4    | 0       | 4   | 1536       |
| 96                   | 128  | 12.288    | 98.304        | 2 | 6.144         | 16      | 16      | 1 | 1024               | 512                | 2    | 49.152        | 64                 | 6144        | 16   | 4    | 0       | 4   | 1536       |
| 96                   | 192  | 18.432    | 98.304        | 3 | 6.144         | 16      | 16      | 1 | 1024               | 512                | 2    | 49.152        | 64                 | 6144        | 16   | 4    | 0       | 4   | 1536       |
| 96                   | 256  | 24.576    | 98.304        | 4 | 6.144         | 16      | 16      | 1 | 1024               | 512                | 2    | 49.152        | 64                 | 6144        | 16   | 4    | 0       | 4   | 1536       |
| 96                   | 384  | 36.864    | 98.304        | 6 | 6.144         | 16      | 16      | 1 | 1024               | 512                | 2    | 49.152        | 64                 | 6144        | 16   | 4    | 0       | 4   | 1536       |
| 96                   | 512  | 49.152    | 98.304        | 8 | 6.144         | 16      | 16      | 1 | 1024               | 512                | 2    | 49.152        | 64                 | 6144        | 16   | 4    | 0       | 4   | 1536       |
| 192                  | 32   | 6.144     | 98.304        | 1 | 6.144         | 16      | 8       | 2 | 512                | 256                | 2    | 49.152        | 32                 | 6144        | 16   | 2    | 0       | 4   | 1536       |
| 192                  | 48   | 9.216     | 98.304        | 3 | 3.072         | 32      | 16      | 2 | 512                | 256                | 2    | 49.152        | 32                 | 6144        | 16   | 2    | 0       | 4   | 1536       |
| 192                  | 64   | 12.288    | 98.304        | 1 | 12.288        | 8       | 4       | 2 | 512                | 256                | 2    | 49.152        | 32                 | 6144        | 16   | 2    | 0       | 4   | 1536       |
| 192                  | 128  | 24.576    | 98.304        | 2 | 12.288        | 8       | 8       | 1 | 512                | 256                | 2    | 49.152        | 32                 | 6144        | 16   | 2    | 0       | 4   | 1536       |
| 192                  | 192  | 36.864    | 98.304        | 3 | 12.288        | 8       | 8       | 1 | 512                | 256                | 2    | 49.152        | 32                 | 6144        | 16   | 2    | 0       | 4   | 1536       |
| 192                  | 256  | 49.152    | 98.304        | 4 | 12.288        | 8       | 8       | 1 | 512                | 256                | 2    | 49.152        | 32                 | 6144        | 16   | 2    | 0       | 4   | 1536       |
| 384                  | 32   | 12.288    | 98.304        | 2 | 6.144         | 16      | 8       | 2 | 256                | 128                | 2    | 49.152        | 16                 | 6144        | 16   | 1    | 0       | 4   | 1536       |
| 384                  | 48   | 18.432    | 98.304        | 3 | 6.144         | 16      | 8       | 2 | 256                | 128                | 2    | 49.152        | 16                 | 6144        | 16   | 1    | 0       | 4   | 1536       |
| 384                  | 64   | 24.576    | 98.304        | 2 | 12.288        | 8       | 4       | 2 | 256                | 128                | 2    | 49.152        | 16                 | 6144        | 16   | 1    | 0       | 4   | 1536       |
| 384                  | 128  | 49.152    | 98.304        | 4 | 12.288        | 8       | 8       | 1 | 256                | 128                | 2    | 49.152        | 16                 | 6144        | 16   | 1    | 0       | 4   | 1536       |

**Table 13. Recommended Clock Divider Settings for PLL as Master Clock (VCOM Mode)**

| f <sub>s</sub> (kHz) | RSCK | SCK (MHz) | PLL VCO (MHz) | P  | PLL REF (MHz) | M = K*R | K = J.D | R | PLL FS | DSP FS | NMAC | DSP CLK (MHz) | MOD f <sub>s</sub> | MOD f (kHz) | NDAC | DOSR | % Error | NCP | CP f (kHz) |
|----------------------|------|-----------|---------------|----|---------------|---------|---------|---|--------|--------|------|---------------|--------------------|-------------|------|------|---------|-----|------------|
| 8                    | 128  | 1.024     | 73.728        | 1  | 1.024         | 72      | 36      | 2 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 8                    | 192  | 1.536     | 73.728        | 1  | 1.536         | 48      | 24      | 2 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 8                    | 256  | 2.048     | 73.728        | 1  | 2.048         | 36      | 36      | 1 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 8                    | 384  | 3.072     | 73.728        | 1  | 3.072         | 24      | 12      | 2 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 8                    | 512  | 4.096     | 73.728        | 2  | 2.048         | 36      | 36      | 1 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 8                    | 768  | 6.144     | 73.728        | 3  | 2.048         | 36      | 36      | 1 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 8                    | 1024 | 8.192     | 73.728        | 4  | 2.048         | 36      | 36      | 1 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 8                    | 1152 | 9.216     | 73.728        | 6  | 1.536         | 48      | 48      | 1 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 8                    | 1536 | 12.288    | 73.728        | 6  | 2.048         | 36      | 36      | 1 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 8                    | 2048 | 16.384    | 73.728        | 8  | 2.048         | 36      | 36      | 1 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 8                    | 3072 | 24.576    | 73.728        | 12 | 2.048         | 36      | 36      | 1 | 9216   | 768    | 12   | 6.144         | 768                | 6144        | 12   | 48   | 0       | 4   | 1536       |
| 11.025               | 128  | 1.4112    | 84.672        | 1  | 1.411         | 60      | 30      | 2 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 192  | 2.1168    | 84.672        | 1  | 2.117         | 40      | 10      | 4 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 256  | 2.8224    | 84.672        | 1  | 2.822         | 30      | 30      | 1 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 384  | 4.2336    | 84.672        | 2  | 2.117         | 40      | 20      | 2 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 512  | 5.6448    | 84.672        | 2  | 2.822         | 30      | 30      | 1 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 768  | 8.4672    | 84.672        | 3  | 2.822         | 30      | 30      | 1 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 1024 | 11.2896   | 84.672        | 4  | 2.822         | 30      | 30      | 1 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 1152 | 12.7008   | 84.672        | 6  | 2.117         | 40      | 20      | 2 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 1536 | 16.9344   | 84.672        | 8  | 2.117         | 40      | 40      | 1 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 2048 | 22.5792   | 84.672        | 8  | 2.822         | 30      | 30      | 1 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 11.025               | 3072 | 33.8688   | 84.672        | 8  | 4.234         | 20      | 20      | 1 | 7680   | 960    | 8    | 10.584        | 512                | 5644.8      | 15   | 32   | 0       | 4   | 1411.2     |
| 16                   | 64   | 1.024     | 73.728        | 1  | 1.024         | 72      | 36      | 2 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 128  | 2.048     | 73.728        | 1  | 2.048         | 36      | 36      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 192  | 3.072     | 73.728        | 1  | 3.072         | 24      | 24      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 256  | 4.096     | 73.728        | 2  | 2.048         | 36      | 36      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 384  | 6.144     | 73.728        | 3  | 2.048         | 36      | 36      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 512  | 8.192     | 73.728        | 4  | 2.048         | 36      | 36      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 768  | 12.288    | 73.728        | 6  | 2.048         | 36      | 36      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 1024 | 16.384    | 73.728        | 8  | 2.048         | 36      | 36      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 1152 | 18.432    | 73.728        | 9  | 2.048         | 36      | 36      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 1536 | 24.576    | 73.728        | 8  | 3.072         | 24      | 24      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 2048 | 32.768    | 73.728        | 8  | 4.096         | 18      | 18      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 16                   | 3072 | 49.152    | 73.728        | 8  | 6.144         | 12      | 12      | 1 | 4608   | 768    | 6    | 12.288        | 384                | 6144        | 12   | 24   | 0       | 4   | 1536       |
| 22.05                | 64   | 1.4112    | 84.672        | 1  | 1.411         | 60      | 30      | 2 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 128  | 2.8224    | 84.672        | 1  | 2.822         | 30      | 30      | 1 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 192  | 4.2336    | 84.672        | 3  | 1.411         | 60      | 30      | 2 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 256  | 5.6448    | 84.672        | 2  | 2.822         | 30      | 30      | 1 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |

**Table 13. Recommended Clock Divider Settings for PLL as Master Clock (VCOM Mode) (continued)**

| f <sub>s</sub> (kHz) | RSCK | SCK (MHz) | PLL VCO (MHz) | P  | PLL REF (MHz) | M = K*R | K = J.D | R | PLL FS | DSP FS | NMAC | DSP CLK (MHz) | MOD f <sub>s</sub> | MOD f (kHz) | NDAC | DOSR | % Error | NCP | CP f (kHz) |
|----------------------|------|-----------|---------------|----|---------------|---------|---------|---|--------|--------|------|---------------|--------------------|-------------|------|------|---------|-----|------------|
| 22.05                | 384  | 8.4672    | 84.672        | 3  | 2.822         | 30      | 30      | 1 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 512  | 11.2896   | 84.672        | 2  | 5.645         | 15      | 15      | 1 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 768  | 16.9344   | 84.672        | 3  | 5.645         | 15      | 15      | 1 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 1024 | 22.5792   | 84.672        | 4  | 5.645         | 15      | 15      | 1 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 1152 | 25.4016   | 84.672        | 9  | 2.822         | 30      | 30      | 1 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 1536 | 33.8688   | 84.672        | 8  | 4.234         | 20      | 20      | 1 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |
| 22.05                | 2048 | 45.1584   | 84.672        | 8  | 5.645         | 15      | 15      | 1 | 3840   | 960    | 4    | 21.168        | 256                | 5644.8      | 15   | 16   | 0       | 4   | 1411.2     |
| 32                   | 32   | 1.024     | 73.728        | 1  | 1.024         | 72      | 36      | 2 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 48   | 1.536     | 73.728        | 1  | 1.536         | 48      | 12      | 4 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 64   | 2.048     | 73.728        | 1  | 2.048         | 36      | 18      | 2 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 128  | 4.096     | 73.728        | 2  | 2.048         | 36      | 36      | 1 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 192  | 6.144     | 73.728        | 3  | 2.048         | 36      | 36      | 1 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 256  | 8.192     | 73.728        | 4  | 2.048         | 36      | 36      | 1 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 384  | 12.288    | 73.728        | 6  | 2.048         | 36      | 36      | 1 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 512  | 16.384    | 73.728        | 8  | 2.048         | 36      | 36      | 1 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 768  | 24.576    | 73.728        | 6  | 4.096         | 18      | 18      | 1 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 1024 | 32.768    | 73.728        | 8  | 4.096         | 18      | 18      | 1 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 1152 | 36.864    | 73.728        | 9  | 4.096         | 18      | 18      | 1 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 32                   | 1536 | 49.152    | 73.728        | 12 | 4.096         | 18      | 18      | 1 | 2304   | 768    | 3    | 24.576        | 192                | 6144        | 12   | 12   | 0       | 4   | 1536       |
| 44.1                 | 32   | 1.4112    | 84.672        | 1  | 1.411         | 60      | 30      | 2 | 1920   | 960    | 2    | 42.336        | 128                | 5644.8      | 15   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 48   | 2.1168    | 84.672        | 1  | 2.117         | 40      | 10      | 4 | 1920   | 960    | 2    | 42.336        | 128                | 5644.8      | 15   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 64   | 2.8224    | 84.672        | 1  | 2.822         | 30      | 15      | 2 | 1920   | 960    | 2    | 42.336        | 128                | 5644.8      | 15   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 128  | 5.6448    | 84.672        | 1  | 5.645         | 15      | 15      | 1 | 1920   | 960    | 2    | 42.336        | 128                | 5644.8      | 15   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 192  | 8.4672    | 84.672        | 2  | 4.234         | 20      | 20      | 1 | 1920   | 960    | 2    | 42.336        | 128                | 5644.8      | 15   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 256  | 11.2896   | 84.672        | 2  | 5.645         | 15      | 15      | 1 | 1920   | 960    | 2    | 42.336        | 128                | 5644.8      | 15   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 384  | 16.9344   | 84.672        | 3  | 5.645         | 15      | 15      | 1 | 1920   | 960    | 2    | 42.336        | 128                | 5644.8      | 15   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 512  | 22.5792   | 84.672        | 4  | 5.645         | 15      | 15      | 1 | 1920   | 960    | 2    | 42.336        | 128                | 5644.8      | 15   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 768  | 33.8688   | 84.672        | 6  | 5.645         | 15      | 15      | 1 | 1920   | 960    | 2    | 42.336        | 128                | 5644.8      | 15   | 8    | 0       | 4   | 1411.2     |
| 44.1                 | 1024 | 45.1584   | 84.672        | 8  | 5.645         | 15      | 15      | 1 | 1920   | 960    | 2    | 42.336        | 128                | 5644.8      | 15   | 8    | 0       | 4   | 1411.2     |
| 48                   | 32   | 1.536     | 73.728        | 1  | 1.536         | 48      | 24      | 2 | 1536   | 768    | 2    | 36.864        | 128                | 6144        | 12   | 8    | 0       | 4   | 1536       |
| 48                   | 48   | 2.304     | 73.728        | 1  | 2.304         | 32      | 8       | 4 | 1536   | 768    | 2    | 36.864        | 128                | 6144        | 12   | 8    | 0       | 4   | 1536       |
| 48                   | 64   | 3.072     | 73.728        | 1  | 3.072         | 24      | 12      | 2 | 1536   | 768    | 2    | 36.864        | 128                | 6144        | 12   | 8    | 0       | 4   | 1536       |
| 48                   | 128  | 6.144     | 73.728        | 2  | 3.072         | 24      | 24      | 1 | 1536   | 768    | 2    | 36.864        | 128                | 6144        | 12   | 8    | 0       | 4   | 1536       |
| 48                   | 192  | 9.216     | 73.728        | 3  | 3.072         | 24      | 24      | 1 | 1536   | 768    | 2    | 36.864        | 128                | 6144        | 12   | 8    | 0       | 4   | 1536       |
| 48                   | 256  | 12.288    | 73.728        | 4  | 3.072         | 24      | 24      | 1 | 1536   | 768    | 2    | 36.864        | 128                | 6144        | 12   | 8    | 0       | 4   | 1536       |
| 48                   | 384  | 18.432    | 73.728        | 6  | 3.072         | 24      | 24      | 1 | 1536   | 768    | 2    | 36.864        | 128                | 6144        | 12   | 8    | 0       | 4   | 1536       |
| 48                   | 512  | 24.576    | 73.728        | 4  | 6.144         | 12      | 12      | 1 | 1536   | 768    | 2    | 36.864        | 128                | 6144        | 12   | 8    | 0       | 4   | 1536       |
| 48                   | 768  | 36.864    | 73.728        | 6  | 6.144         | 12      | 12      | 1 | 1536   | 768    | 2    | 36.864        | 128                | 6144        | 12   | 8    | 0       | 4   | 1536       |

**Table 13. Recommended Clock Divider Settings for PLL as Master Clock (VCOM Mode) (continued)**

| $f_s$ (kHz) | RSCK | SCK (MHz) | PLL VCO (MHz) | P | PLL REF (MHz) | M = K*R | K = J.D | R | PLL FS | DSP FS | NMAC | DSP CLK (MHz) | MOD $f_s$ | MOD f (kHz) | NDAC | DOSR | % Error | NCP | CP f (kHz) |
|-------------|------|-----------|---------------|---|---------------|---------|---------|---|--------|--------|------|---------------|-----------|-------------|------|------|---------|-----|------------|
| 48          | 1024 | 49.152    | 73.728        | 8 | 6.144         | 12      | 12      | 1 | 1536   | 768    | 2    | 36.864        | 128       | 6144        | 12   | 8    | 0       | 4   | 1536       |
| 96          | 32   | 3.072     | 73.728        | 2 | 1.536         | 48      | 24      | 2 | 768    | 384    | 2    | 36.864        | 64        | 6144        | 12   | 4    | 0       | 4   | 1536       |
| 96          | 48   | 4.608     | 73.728        | 3 | 1.536         | 48      | 24      | 2 | 768    | 384    | 2    | 36.864        | 64        | 6144        | 12   | 4    | 0       | 4   | 1536       |
| 96          | 64   | 6.144     | 73.728        | 2 | 3.072         | 24      | 12      | 2 | 768    | 384    | 2    | 36.864        | 64        | 6144        | 12   | 4    | 0       | 4   | 1536       |
| 96          | 128  | 12.288    | 73.728        | 4 | 3.072         | 24      | 24      | 1 | 768    | 384    | 2    | 36.864        | 64        | 6144        | 12   | 4    | 0       | 4   | 1536       |
| 96          | 192  | 18.432    | 73.728        | 6 | 3.072         | 24      | 24      | 1 | 768    | 384    | 2    | 36.864        | 64        | 6144        | 12   | 4    | 0       | 4   | 1536       |
| 96          | 256  | 24.576    | 73.728        | 8 | 3.072         | 24      | 24      | 1 | 768    | 384    | 2    | 36.864        | 64        | 6144        | 12   | 4    | 0       | 4   | 1536       |
| 96          | 384  | 36.864    | 73.728        | 6 | 6.144         | 12      | 12      | 1 | 768    | 384    | 2    | 36.864        | 64        | 6144        | 12   | 4    | 0       | 4   | 1536       |
| 96          | 512  | 49.152    | 73.728        | 8 | 6.144         | 12      | 12      | 1 | 768    | 384    | 2    | 36.864        | 64        | 6144        | 12   | 4    | 0       | 4   | 1536       |
| 192         | 32   | 6.144     | 73.728        | 2 | 3.072         | 24      | 12      | 2 | 384    | 192    | 2    | 36.864        | 32        | 6144        | 12   | 2    | 0       | 4   | 1536       |
| 192         | 48   | 9.216     | 73.728        | 3 | 3.072         | 24      | 12      | 2 | 384    | 192    | 2    | 36.864        | 32        | 6144        | 12   | 2    | 0       | 4   | 1536       |
| 192         | 64   | 12.288    | 73.728        | 4 | 3.072         | 24      | 12      | 2 | 384    | 192    | 2    | 36.864        | 32        | 6144        | 12   | 2    | 0       | 4   | 1536       |
| 192         | 128  | 24.576    | 73.728        | 8 | 3.072         | 24      | 24      | 1 | 384    | 192    | 2    | 36.864        | 32        | 6144        | 12   | 2    | 0       | 4   | 1536       |
| 192         | 192  | 36.864    | 73.728        | 6 | 6.144         | 12      | 12      | 1 | 384    | 192    | 2    | 36.864        | 32        | 6144        | 12   | 2    | 0       | 4   | 1536       |
| 192         | 256  | 49.152    | 73.728        | 8 | 6.144         | 12      | 12      | 1 | 384    | 192    | 2    | 36.864        | 32        | 6144        | 12   | 2    | 0       | 4   | 1536       |
| 384         | 32   | 12.288    | 73.728        | 2 | 6.144         | 12      | 6       | 2 | 192    | 96     | 2    | 36.864        | 16        | 6144        | 12   | 1    | 0       | 4   | 1536       |
| 384         | 48   | 18.432    | 73.728        | 3 | 6.144         | 12      | 6       | 2 | 192    | 96     | 2    | 36.864        | 16        | 6144        | 12   | 1    | 0       | 4   | 1536       |
| 384         | 64   | 24.576    | 73.728        | 4 | 6.144         | 12      | 6       | 2 | 192    | 96     | 2    | 36.864        | 16        | 6144        | 12   | 1    | 0       | 4   | 1536       |
| 384         | 128  | 49.152    | 73.728        | 8 | 6.144         | 12      | 12      | 1 | 192    | 96     | 2    | 36.864        | 16        | 6144        | 12   | 1    | 0       | 4   | 1536       |

**Table 14. Recommended Clock Divider Settings for SCK as Master Clock**

| f <sub>s</sub> (kHz) | RSCK | SCK (MHz) | DSP f <sub>s</sub> | NMAC | DSP CLK (MHz) | MOD f <sub>s</sub> | MOD f (kHz) | NDAC | DOSR | NCP | CP f (kHz) |
|----------------------|------|-----------|--------------------|------|---------------|--------------------|-------------|------|------|-----|------------|
| 8                    | 256  | 2.048     | 256                | 1    | 2.048         | 256                | 2048        | 1    | 16   | 2   | 1024       |
| 8                    | 384  | 3.072     | 384                | 1    | 3.072         | 384                | 3072        | 1    | 24   | 2   | 1536       |
| 8                    | 512  | 4.096     | 512                | 1    | 4.096         | 512                | 4096        | 1    | 32   | 2   | 2048       |
| 8                    | 768  | 6.144     | 768                | 1    | 6.144         | 768                | 6144        | 1    | 48   | 4   | 1536       |
| 8                    | 1024 | 8.192     | 1024               | 1    | 8.192         | 512                | 4096        | 2    | 32   | 2   | 2048       |
| 8                    | 1152 | 9.216     | 1152               | 1    | 9.216         | 576                | 4608        | 2    | 36   | 4   | 1152       |
| 8                    | 1536 | 12.288    | 1536               | 1    | 12.288        | 768                | 6144        | 2    | 48   | 4   | 1536       |
| 8                    | 2048 | 16.384    | 2048               | 1    | 16.384        | 512                | 4096        | 4    | 32   | 2   | 2048       |
| 8                    | 3072 | 24.576    | 3072               | 1    | 24.576        | 768                | 6144        | 4    | 48   | 4   | 1536       |
| 11.025               | 256  | 2.8224    | 256                | 1    | 2.822         | 256                | 2822.4      | 1    | 16   | 2   | 1411.2     |
| 11.025               | 384  | 4.2336    | 384                | 1    | 4.234         | 384                | 4233.6      | 1    | 24   | 4   | 1058.4     |
| 11.025               | 1152 | 12.7008   | 1152               | 1    | 12.701        | 384                | 4233.6      | 3    | 24   | 4   | 1058.4     |
| 11.025               | 1536 | 16.9344   | 1536               | 1    | 16.934        | 512                | 5644.8      | 3    | 32   | 4   | 1411.2     |
| 11.025               | 2048 | 22.5792   | 2048               | 1    | 22.579        | 512                | 5644.8      | 4    | 32   | 4   | 1411.2     |
| 11.025               | 3072 | 33.8688   | 3072               | 1    | 33.869        | 512                | 5644.8      | 6    | 32   | 4   | 1411.2     |
| 16                   | 256  | 4.096     | 256                | 1    | 4.096         | 256                | 4096        | 1    | 16   | 2   | 2048       |
| 16                   | 384  | 6.144     | 384                | 1    | 6.144         | 384                | 6144        | 1    | 24   | 4   | 1536       |
| 16                   | 512  | 8.192     | 512                | 1    | 8.192         | 256                | 4096        | 2    | 16   | 2   | 2048       |
| 16                   | 768  | 12.288    | 768                | 1    | 12.288        | 384                | 6144        | 2    | 24   | 4   | 1536       |
| 16                   | 1152 | 18.432    | 1152               | 1    | 18.432        | 288                | 4608        | 4    | 18   | 4   | 1152       |
| 16                   | 1536 | 24.576    | 1536               | 1    | 24.576        | 384                | 6144        | 4    | 24   | 4   | 1536       |
| 16                   | 2048 | 32.768    | 2048               | 1    | 32.768        | 256                | 4096        | 8    | 16   | 2   | 2048       |
| 16                   | 3072 | 49.152    | 3072               | 1    | 49.152        | 384                | 6144        | 8    | 24   | 4   | 1536       |
| 22.05                | 256  | 5.6448    | 256                | 1    | 5.645         | 256                | 5644.8      | 1    | 16   | 4   | 1411.2     |
| 22.05                | 384  | 8.4672    | 384                | 1    | 8.467         | 192                | 4233.6      | 2    | 12   | 4   | 1058.4     |
| 22.05                | 512  | 11.2896   | 512                | 1    | 11.29         | 256                | 5644.8      | 2    | 16   | 4   | 1411.2     |
| 22.05                | 768  | 16.9344   | 768                | 1    | 16.934        | 256                | 5644.8      | 3    | 16   | 4   | 1411.2     |
| 22.05                | 1024 | 22.5792   | 1024               | 1    | 22.579        | 256                | 5644.8      | 4    | 16   | 4   | 1411.2     |
| 22.05                | 1152 | 25.4016   | 1152               | 1    | 25.402        | 192                | 4233.6      | 6    | 12   | 4   | 1058.4     |
| 22.05                | 1536 | 33.8688   | 1536               | 1    | 33.869        | 256                | 5644.8      | 6    | 16   | 4   | 1411.2     |
| 22.05                | 2048 | 45.1584   | 2048               | 1    | 45.158        | 256                | 5644.8      | 8    | 16   | 4   | 1411.2     |
| 32                   | 256  | 8.192     | 256                | 1    | 8.192         | 128                | 4096        | 2    | 8    | 2   | 2048       |
| 32                   | 384  | 12.288    | 384                | 1    | 12.288        | 128                | 4096        | 3    | 8    | 2   | 2048       |
| 32                   | 512  | 16.384    | 512                | 1    | 16.384        | 128                | 4096        | 4    | 8    | 2   | 2048       |
| 32                   | 768  | 24.576    | 768                | 1    | 24.576        | 128                | 4096        | 6    | 8    | 2   | 2048       |
| 32                   | 1024 | 32.768    | 1024               | 1    | 32.768        | 128                | 4096        | 8    | 8    | 2   | 2048       |
| 32                   | 1152 | 36.864    | 1152               | 1    | 36.864        | 128                | 4096        | 9    | 8    | 4   | 1024       |
| 32                   | 1536 | 49.152    | 1536               | 1    | 49.152        | 128                | 4096        | 12   | 8    | 4   | 1024       |
| 44.1                 | 256  | 11.2896   | 256                | 1    | 11.29         | 128                | 5644.8      | 2    | 8    | 4   | 1411.2     |
| 44.1                 | 384  | 16.9344   | 384                | 1    | 16.934        | 128                | 5644.8      | 3    | 8    | 4   | 1411.2     |
| 44.1                 | 512  | 22.5792   | 512                | 1    | 22.579        | 128                | 5644.8      | 4    | 8    | 4   | 1411.2     |
| 44.1                 | 768  | 33.8688   | 768                | 1    | 33.869        | 128                | 5644.8      | 6    | 8    | 4   | 1411.2     |
| 44.1                 | 1024 | 45.1584   | 1024               | 1    | 45.158        | 128                | 5644.8      | 8    | 8    | 4   | 1411.2     |
| 48                   | 256  | 12.288    | 256                | 1    | 12.288        | 128                | 6144        | 2    | 8    | 4   | 1536       |
| 48                   | 384  | 18.432    | 384                | 1    | 18.432        | 128                | 6144        | 3    | 8    | 4   | 1536       |
| 48                   | 512  | 24.576    | 512                | 1    | 24.576        | 128                | 6144        | 4    | 8    | 4   | 1536       |
| 48                   | 768  | 36.864    | 768                | 1    | 36.864        | 128                | 6144        | 6    | 8    | 4   | 1536       |
| 48                   | 1024 | 49.152    | 1024               | 1    | 49.152        | 128                | 6144        | 8    | 8    | 4   | 1536       |
| 96                   | 192  | 18.432    | 192                | 1    | 18.432        | 48                 | 4608        | 4    | 3    | 6   | 768        |
| 96                   | 256  | 24.576    | 256                | 1    | 24.576        | 64                 | 6144        | 4    | 4    | 4   | 1536       |
| 96                   | 384  | 36.864    | 384                | 1    | 36.864        | 64                 | 6144        | 6    | 4    | 4   | 1536       |
| 96                   | 512  | 49.152    | 512                | 1    | 49.152        | 64                 | 6144        | 8    | 4    | 4   | 1536       |

**Table 14. Recommended Clock Divider Settings for SCK as Master Clock (continued)**

| $f_s$ (kHz) | RSCK | SCK (MHz) | DSP $f_s$ | NMAC | DSP CLK (MHz) | MOD $f_s$ | MOD $f$ (kHz) | NDAC | DOSR | NCP | CP $f$ (kHz) |
|-------------|------|-----------|-----------|------|---------------|-----------|---------------|------|------|-----|--------------|
| 192         | 128  | 24.576    | 128       | 1    | 24.576        | 32        | 6144          | 4    | 2    | 4   | 1536         |
| 192         | 192  | 36.864    | 192       | 1    | 36.864        | 32        | 6144          | 6    | 2    | 4   | 1536         |
| 192         | 256  | 49.152    | 256       | 1    | 49.152        | 32        | 6144          | 8    | 2    | 4   | 1536         |
| 384         | 64   | 24.576    | 64        | 1    | 24.576        | 16        | 6144          | 4    | 1    | 4   | 1536         |
| 384         | 128  | 49.152    | 128       | 1    | 49.152        | 16        | 6144          | 8    | 1    | 4   | 1536         |

## Audio Data Interface

### Audio Serial Interface

The audio interface port is a 3-wire serial port with the signals LRCK (pin 15), BCK (pin 13), and DIN (pin 14). BCK is the serial audio bit clock, used to clock the serial data present on DIN into the serial shift register of the audio interface. Serial data is clocked into the PCM512x on the rising edge of BCK. LRCK is the serial audio left/right word clock.

**Table 15. PCM512x Audio Data Formats, Bit Depths and Clock Rates**

| CONTROL MODE                                  | FORMAT              | DATA BITS      | MAX LRCK<br>FREQUENCY [ $f_s$ ] | SCK RATE [ $\times f_s$ ] | BCK RATE [ $\times f_s$ ] |
|-----------------------------------------------|---------------------|----------------|---------------------------------|---------------------------|---------------------------|
| Software Control<br>(SPI or I <sup>2</sup> S) | I <sup>2</sup> S/LJ | 32, 24, 20, 16 | Up to 192kHz                    | 128 – 3072                | 64, 48, 32                |
|                                               |                     |                | 384kHz                          | 64, 128                   | 64, 48, 32                |
|                                               | TDM                 | 32, 24, 20, 16 | Up to 48kHz                     | 128 – 3072                | 125, 256                  |
|                                               |                     |                | 96kHz                           | 128 – 512                 | 125, 256                  |
|                                               |                     |                | 192kHz                          | 128, 192, 256             | 128                       |
| Hardware Control                              | I <sup>2</sup> S/LJ | 32, 24, 20, 16 | Up to 192kHz                    | 128 – 3072                | 64, 48, 32                |
|                                               |                     |                | 384kHz                          | 64, 128                   | 64, 48, 32                |

The PCM512x requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than  $\pm 5$  SCK, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and system clock is completed.

If the relationship between LRCK and BCK are invalid more than 4 LRCK periods, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and BCK is completed.

## PCM Audio Data Formats and Timing

The PCM512x supports industry-standard audio data formats, including standard I<sup>2</sup>S and left-justified. Data formats are selected using the FMT (pin 16), Low for I<sup>2</sup>S, and High for Left-justified. All formats require binary 2s-complement, MSB-first audio data; up to 32-bit audio data is accepted.

The PCM512x also supports right-justified and TDM in software control mode. I<sup>2</sup>S, LJ, RJ, and TDM are selected using Register (Pg0Reg40). All formats require binary 2s complement, MSB-first audio data. Up to 32 bits are accepted. Default setting is I<sup>2</sup>S and 24 bit word length. The I<sup>2</sup>S slave timing is shown in Figure 27.

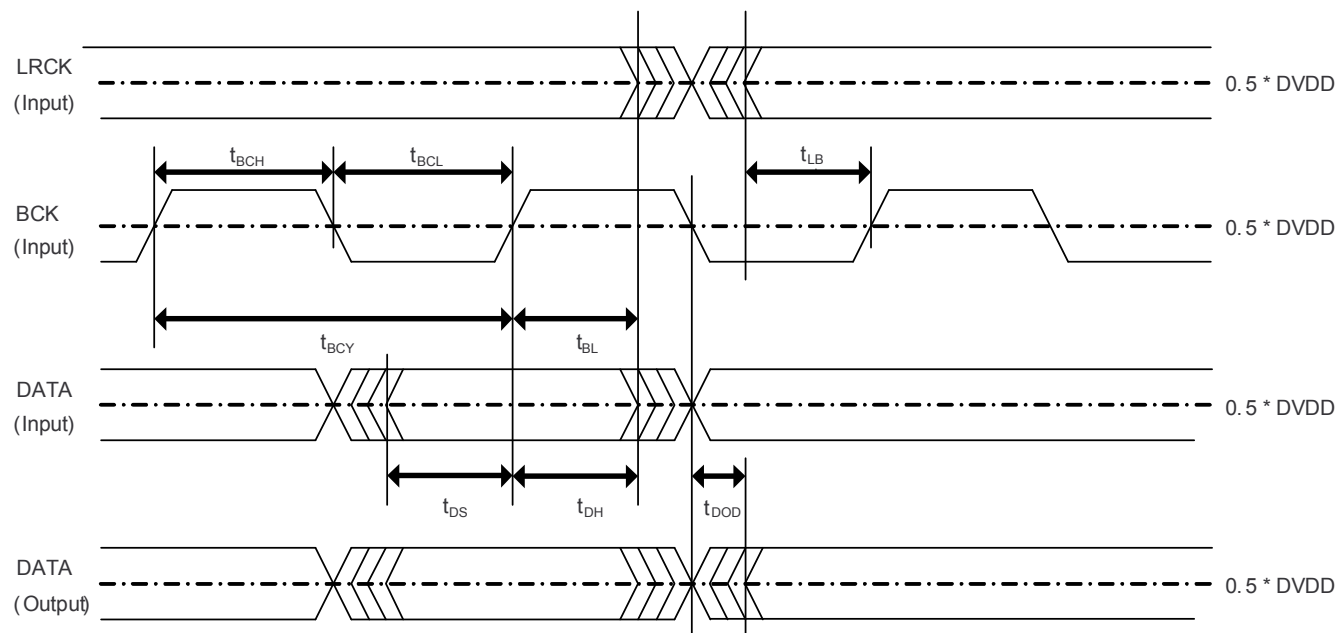


Figure 27. PCM512x Serial Audio Timing - Slave

Table 16. Audio Interface Slave Timing

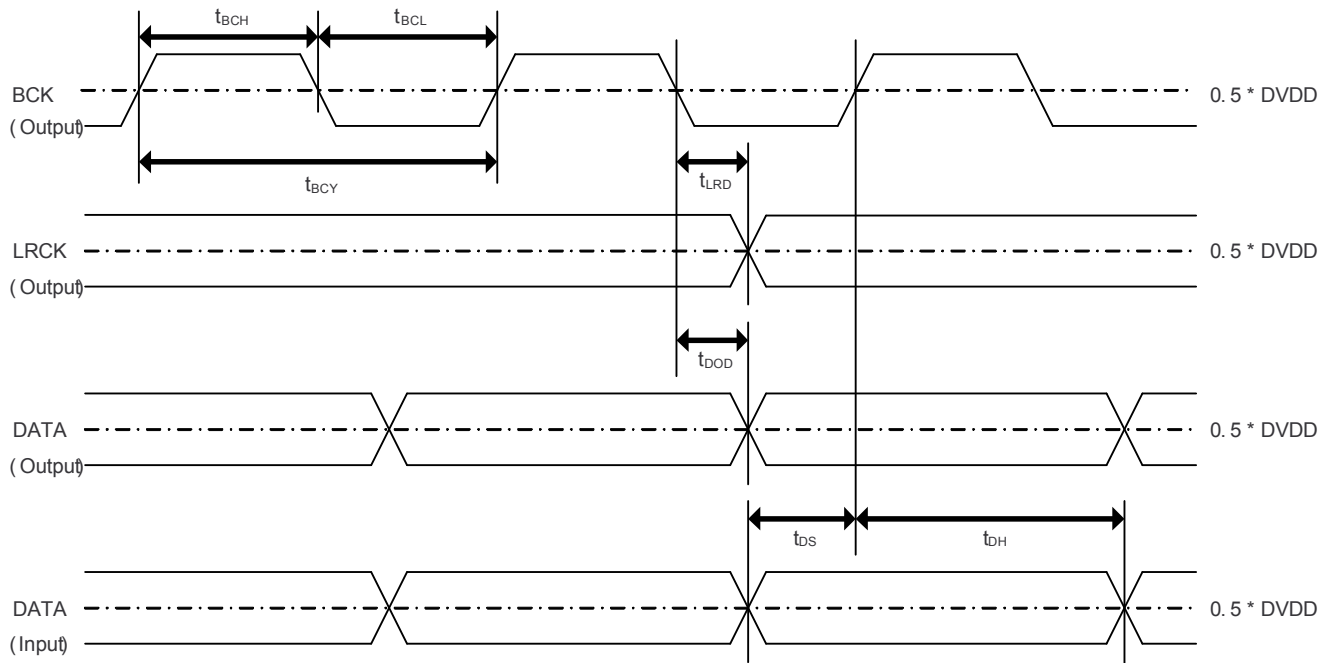
|                 | Parameters                            | Min | Max    | Units |
|-----------------|---------------------------------------|-----|--------|-------|
| $t_{BCY}$       | BCK Pulse Cycle Time                  | 40  |        | ns    |
| $t_{BCL}$       | BCK Pulse Width LOW                   | 16  |        | ns    |
| $t_{BCH}$       | BCK Pulse Width HIGH                  | 16  |        | ns    |
| $t_{BL}$        | BCK Rising Edge to LRCK Edge          | 8   |        | ns    |
| $t_{BCK}$       | BCK frequency at DVDD = 3.3V          |     | 24.576 | MHz   |
| $t_{BCK(1.8V)}$ | BCK frequency at DVDD = 1.8V          |     | 12.288 | MHz   |
| $t_{LB}$        | LRCK Edge to BCK Rising Edge          | 8   |        | ns    |
| $t_{DS}$        | DATA Set Up Time                      | 8   |        | ns    |
| $t_{DH}$        | DATA Hold Time                        | 8   |        | ns    |
| $t_{DOD}$       | DATA delay time from BCK falling edge |     | 15     | ns    |

In software mode, the PCM512x can act as an I<sup>2</sup>S master, generating BCK and LRCK as outputs from the SCK input.

Table 17. I<sup>2</sup>S Master Mode Registers

| Register                                | Function                            |
|-----------------------------------------|-------------------------------------|
| Page0, Register 9, D(0), D(4), and D(5) | I <sup>2</sup> S Master mode select |
| Register 32, D(6:0)                     | BCK divider and LRCK divider        |
| Register 33, D(7:0)                     |                                     |

The I<sup>2</sup>S master timing is shown in Figure 28 and Table 18.



**Figure 28. PCM512x Serial Audio Timing - Master**

**Table 18. Audio Interface Master Timing**

|                 | Parameters                                           | Min | Max    | Units |
|-----------------|------------------------------------------------------|-----|--------|-------|
| $t_{BCY}$       | BCK Pulse Cycle Time                                 | 40  |        | ns    |
| $t_{BCL}$       | BCK Pulse Width LOW                                  | 16  |        | ns    |
| $t_{BCH}$       | BCK Pulse Width HIGH                                 | 16  |        | ns    |
| $t_{BCK}$       | BCK frequency at DVDD = 3.3V                         |     | 24.576 | MHz   |
| $t_{BCK(1.8V)}$ | BCK frequency at DVDD = 1.8V                         |     | 12.288 | MHz   |
| $t_{LRD}$       | LRCKx delay time from BCKx falling edge              | –10 | 20     | ns    |
| $t_{DS}$        | DATA Set Up Time                                     | 8   |        | ns    |
| $t_{DH}$        | DATA Hold Time                                       | 8   |        | ns    |
| $t_{DOD}$       | DATA delay time from BCK falling edge at DVDD = 3.3V |     | 15     | ns    |
| $t_{DOD(1.8V)}$ | DATA delay time from BCK falling edge at DVDD = 1.8V |     | 20     | ns    |

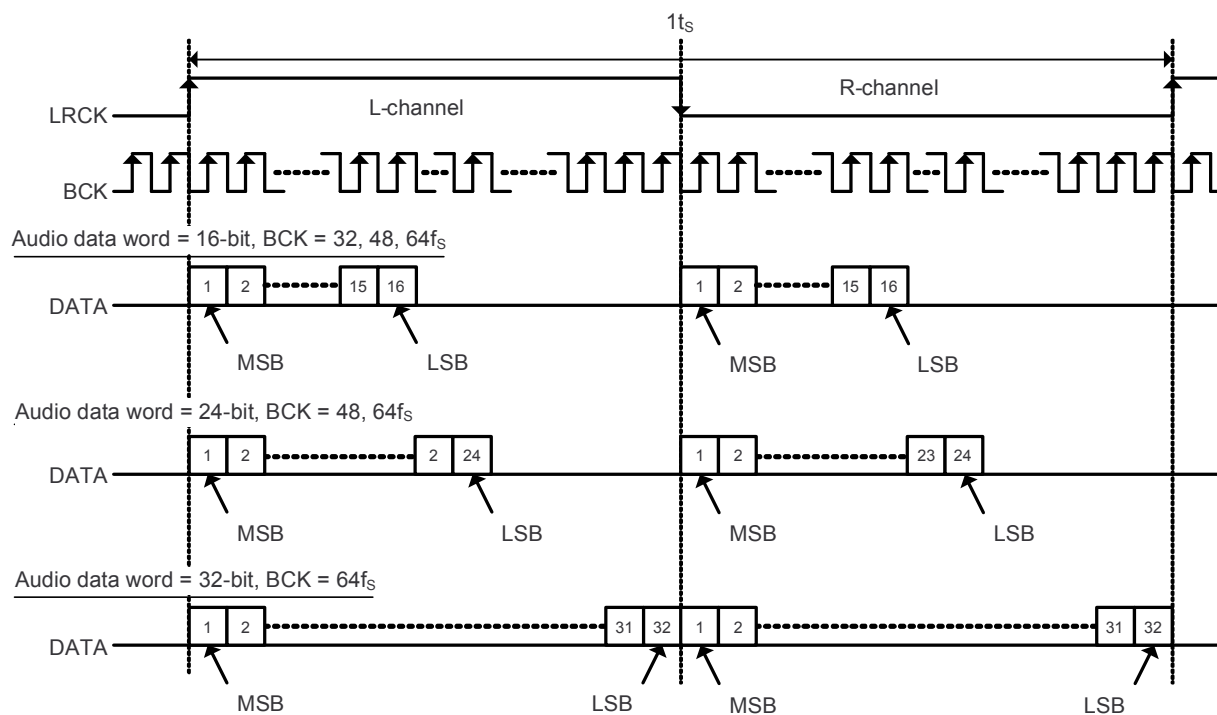
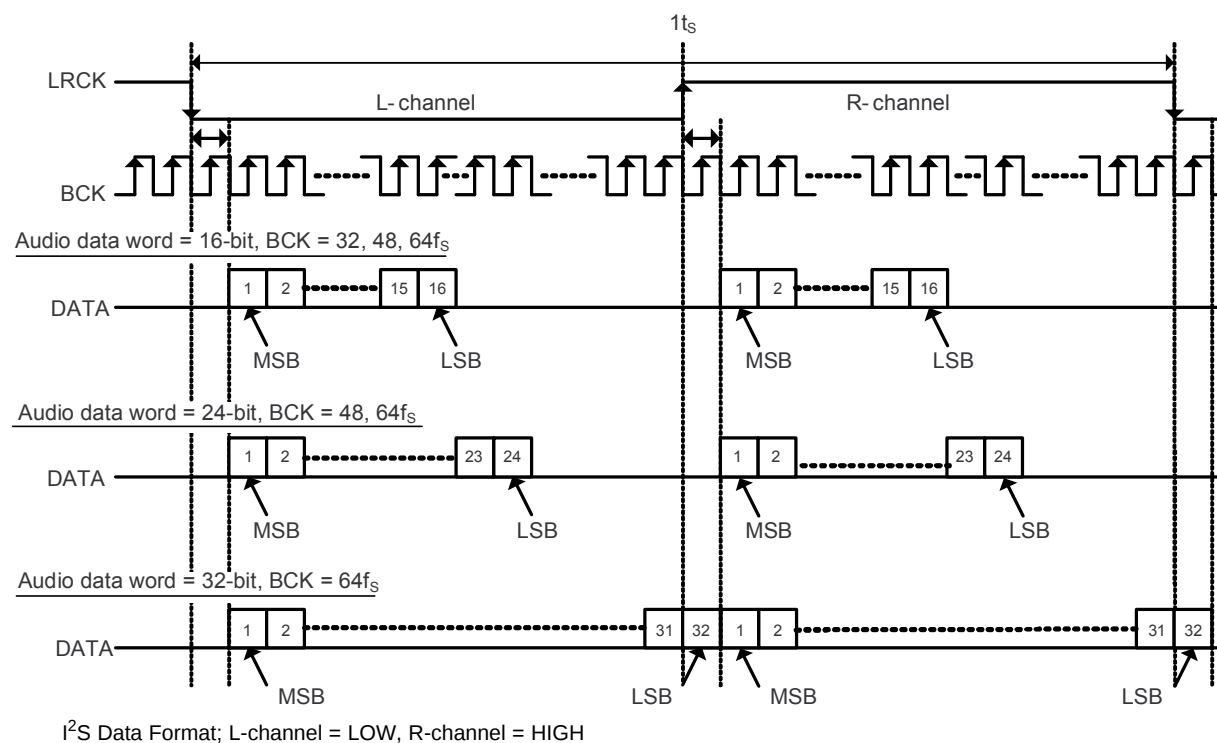
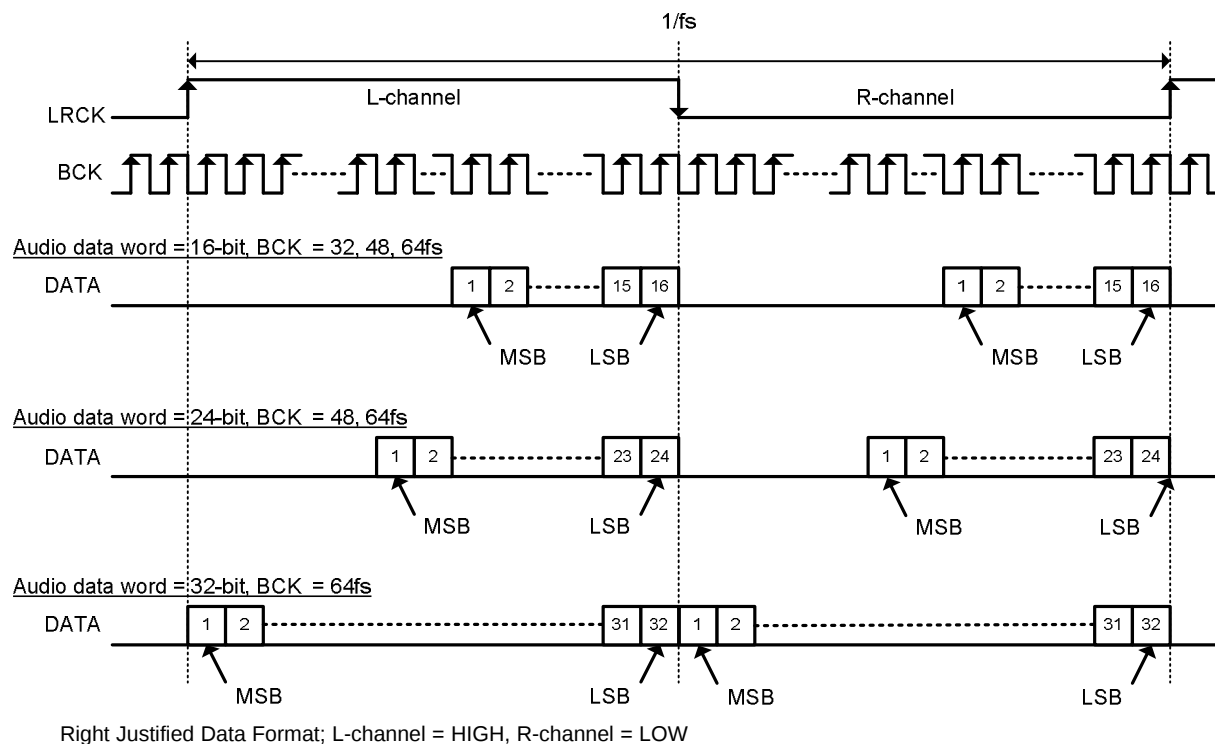


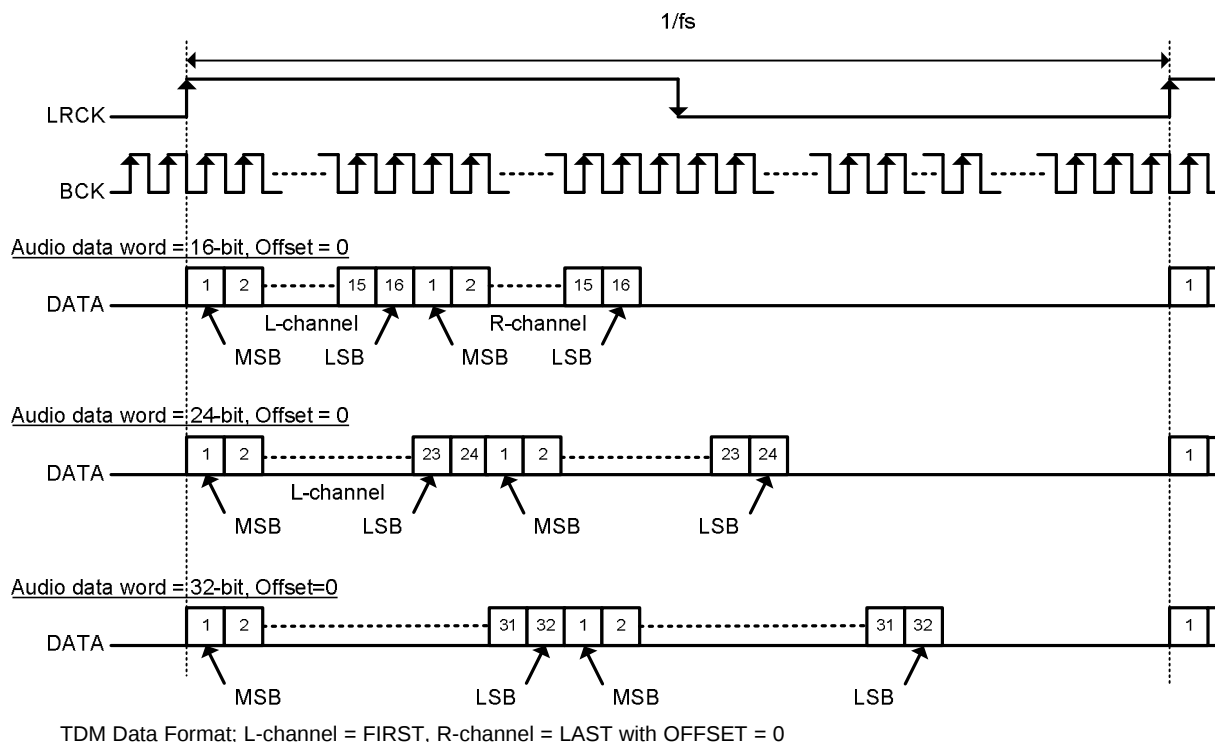
Figure 29. Left Justified Audio Data Format

Figure 30. I<sup>2</sup>S Audio Data Format

The following data formats are only available in software mode.



**Figure 31. Right Justified Audio Data Format**



**Figure 32. TDM 1 Audio Data Format**

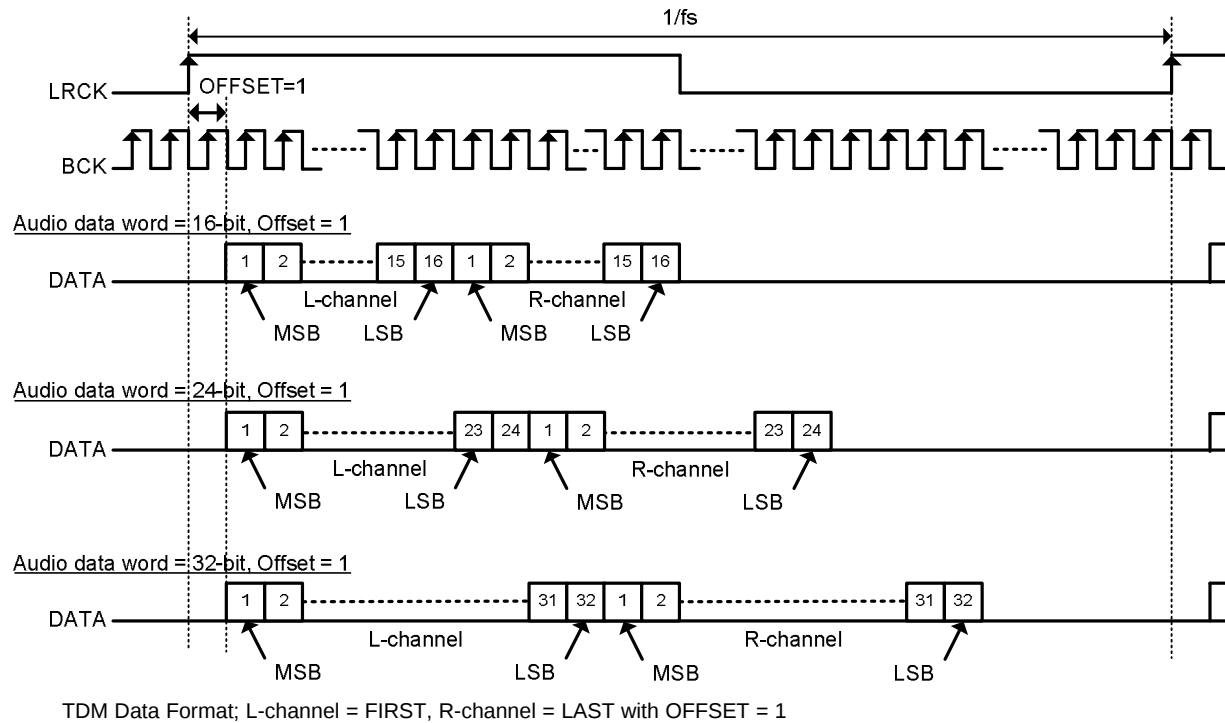


Figure 33. TDM 2 Audio Data Format

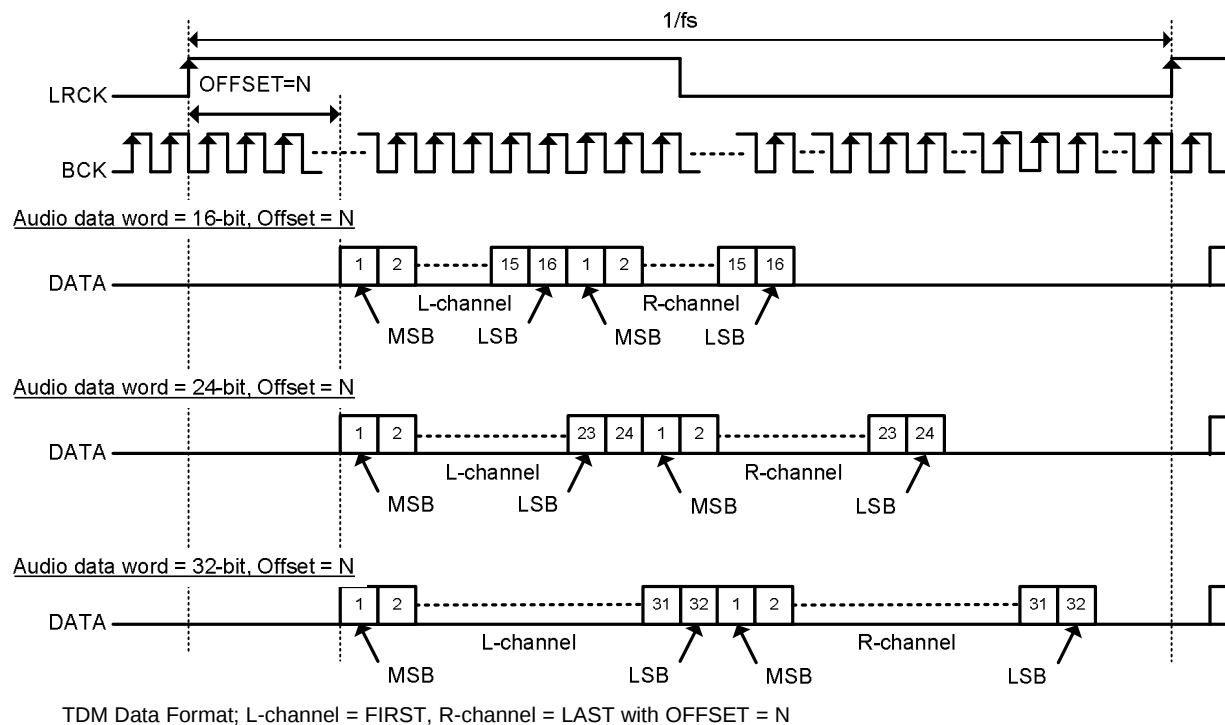


Figure 34. TDM 3 Audio Data Format

## Function Descriptions

### PCM512x Audio Processing

#### Overview

The PCM512x supports a fixed audio processing flow with programmable coefficients. (Program 5 - [Fixed Audio Processing Flow \(Program 5\)](#) of this datasheet). Details can be found below.

#### Software

Software development for the PCM512x is supported through TI's comprehensive PurePath Studio Development Environment; a powerful, easy-to-use tool designed specifically to simplify software development on the PCM512x miniDSP audio platform. The Graphical Development Environment consists of a library of common audio functions that can be dragged-and-dropped into an audio signal flow and graphically connected together. The DSP code can then be assembled from the graphical signal flow with the click of a mouse.

Please visit the PCM512x product folder on [www.ti.com](http://www.ti.com) to learn more about PurePath Studio and the latest status on available, ready-to-use DSP algorithms.

## Interpolation Filter

The PCM512x provides 4 types of interpolation filters, selectable by writing to Page 0, Register 43, D(4:0).

**Table 19. ROM Preset Programs**

| Program number | D(4:0) | Description                                                   | Minimum Cycles |
|----------------|--------|---------------------------------------------------------------|----------------|
| 0              | 0 0000 | Reserved                                                      |                |
| 1              | 0 0001 | Normal x8/x4/x2/x1 Interpolation Filter <sup>(1)</sup>        | 256            |
| 2              | 0 0010 | Low Latency x8/x4/x2/x1 Interpolation Filter <sup>(1)</sup>   | 256            |
| 3              | 0 0011 | High Attenuation x8/x4/x2 Interpolation Filter <sup>(1)</sup> | 512            |
| 4              | 0 0100 | Reserved                                                      |                |
| 5              | 0 0101 | Preset Process Flow                                           | n/a            |
| 6              | 0 0110 | Reserved                                                      |                |
| 7              | 0 0111 | Asymmetric FIR Interpolation Filter <sup>(1)</sup>            | 512            |
| :              | :      | Reserved                                                      |                |
| 31             | 1 1111 | Reserved                                                      |                |

(1)  $f_s$  44.1kHz De-emphasis filter is supported.

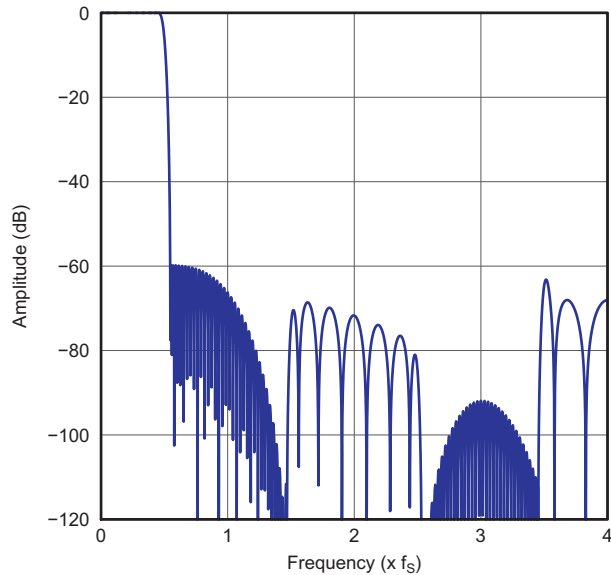
The PCM512x supports four sampling modes (single rate, dual rate, quad rate, and octal rate) which produce different oversampling rates (OSR) in the interpolation digital filter operation. These are shown in [Table 20](#).

**Table 20. Sampling Modes and Oversampling Rates**

| Sampling Mode | Sampling Frequency ( $f_s$ ) kHz | Oversampling Rate (OSR) |
|---------------|----------------------------------|-------------------------|
| Single Rate   | 8                                | 8 or 16                 |
|               | 16                               |                         |
|               | 32                               |                         |
|               | 44.1                             |                         |
|               | 48                               |                         |
| Dual Rate     | 88.2                             | 4                       |
|               | 96                               |                         |
| Quad Rate     | 176.4                            | 2                       |
|               | 192                              |                         |
| Octal Rate    | 384                              | 1 (Bypass)              |

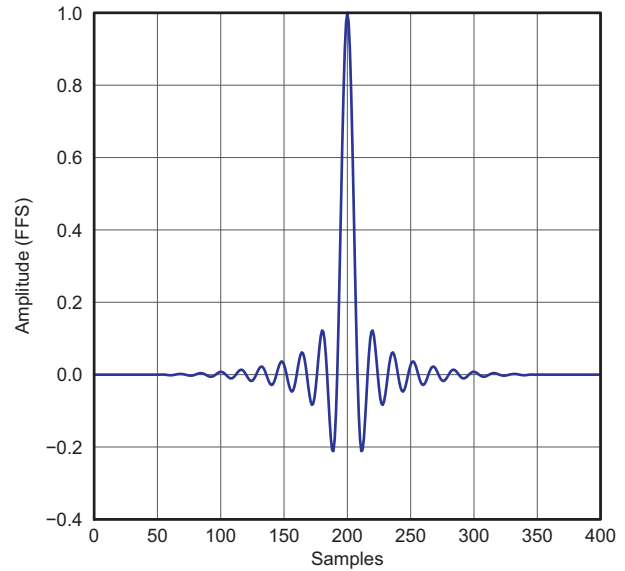
**Table 21. Normal x8 Interpolation Filter, Single Rate**

| Parameter             | Condition                                    | Value (Typical)   | Value (Max) | Units |
|-----------------------|----------------------------------------------|-------------------|-------------|-------|
| Filter Gain Pass Band | 0 ..... 0.45f <sub>S</sub>                   |                   |             | dB    |
| Filter Gain Stop Band | 0.55f <sub>S</sub> ..... 7.455f <sub>S</sub> |                   |             | dB    |
| Filter Group Delay    |                                              | 20/f <sub>S</sub> |             | S     |



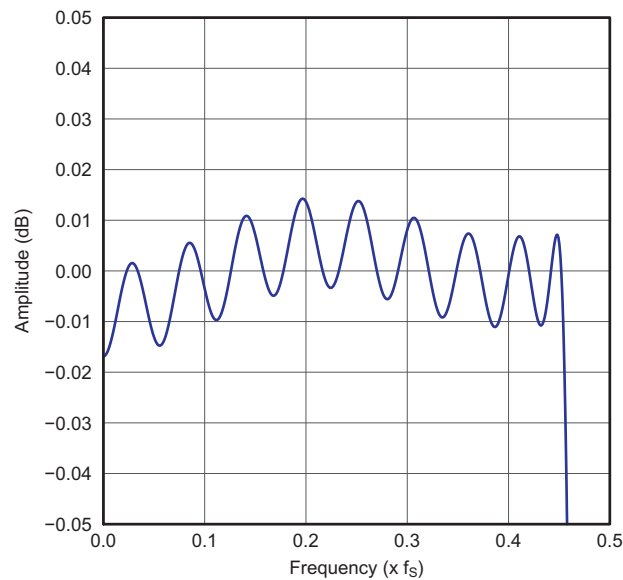
G012

**Figure 35. Normal x8 Interpolation Filter Frequency Response**



G023

**Figure 36. Normal x8 Interpolation Filter Impulse Response**

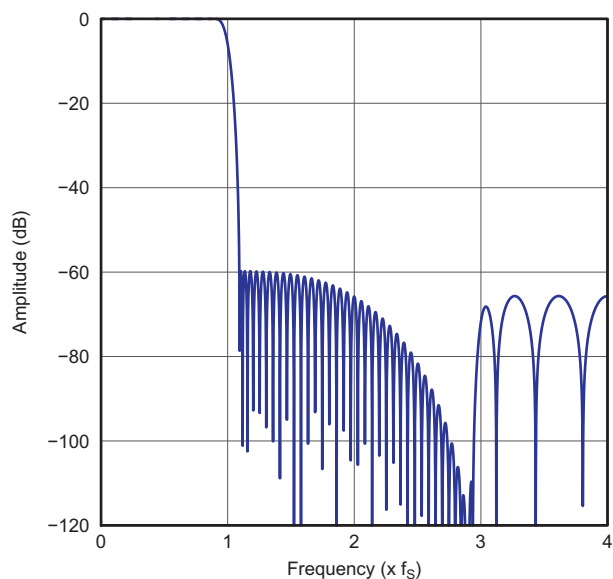


G034

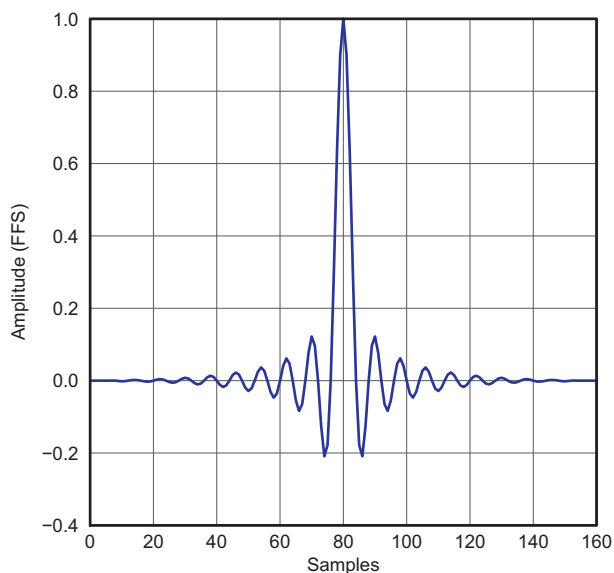
**Figure 37. Normal x8 Interpolation Filter Passband Ripple**

**Table 22. Normal x4 Interpolation Filter, Dual Rate**

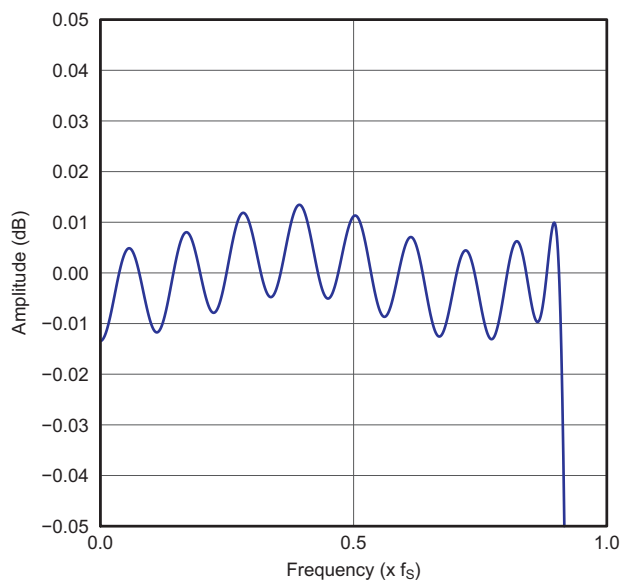
| Parameter             | Condition                                    | Value (Typical)   | Value (Max) | Units |
|-----------------------|----------------------------------------------|-------------------|-------------|-------|
| Filter Gain Pass Band | 0 ..... 0.45f <sub>S</sub>                   |                   |             | dB    |
| Filter Gain Stop Band | 0.55f <sub>S</sub> ..... 3.455f <sub>S</sub> |                   |             | dB    |
| Filter Group Delay    |                                              | 20/f <sub>S</sub> |             | S     |



G009

**Figure 38. Normal x4 Interpolation Filter Frequency Response**

G020

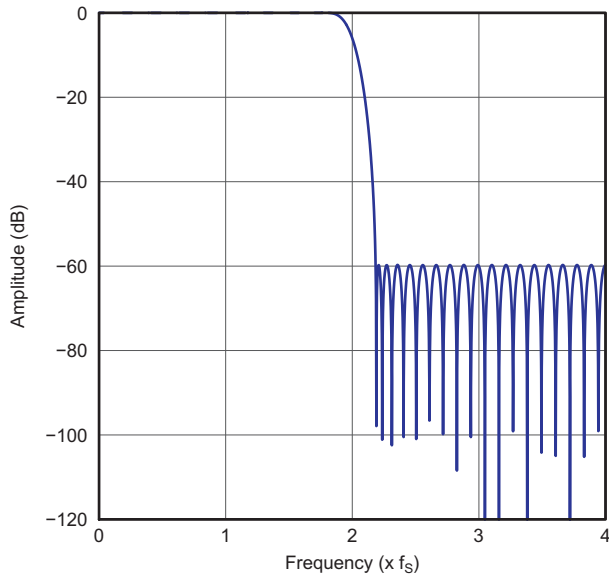
**Figure 39. Normal x4 Interpolation Filter Impulse Response**

G031

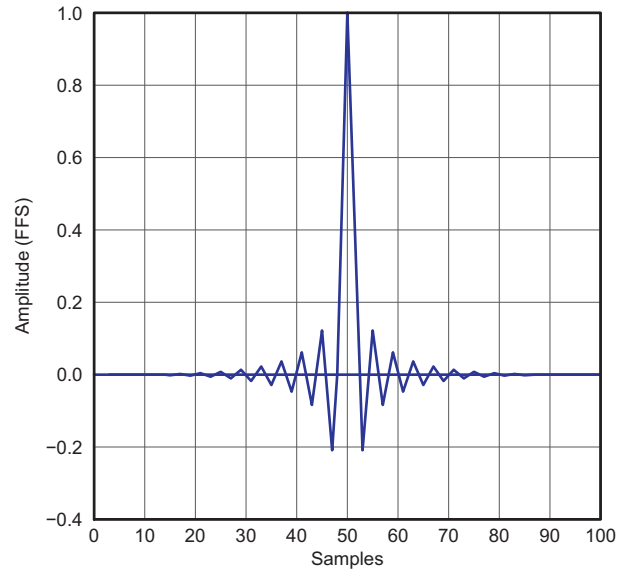
**Figure 40. Normal x4 Interpolation Filter Passband Ripple**

**Table 23. Normal x2 Interpolation Filter, Quad Rate**

| Parameter             | Condition                                    | Value (Typical)   | Value (Max) | Units |
|-----------------------|----------------------------------------------|-------------------|-------------|-------|
| Filter Gain Pass Band | 0 ..... 0.45f <sub>S</sub>                   |                   |             | dB    |
| Filter Gain Stop Band | 0.55f <sub>S</sub> ..... 1.455f <sub>S</sub> |                   |             | dB    |
| Filter Group Delay    |                                              | 20/f <sub>S</sub> |             | S     |



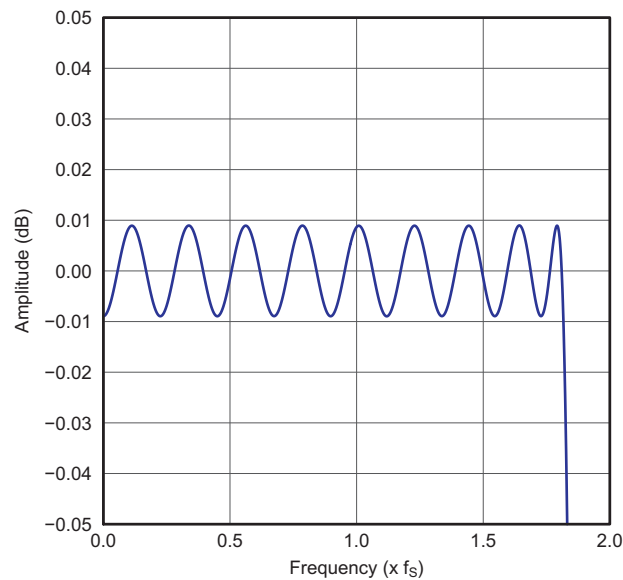
G006



G017

**Figure 41. Normal x2 Interpolation Filter Frequency Response**

**Figure 42. Normal x2 Interpolation Filter Impulse Response**

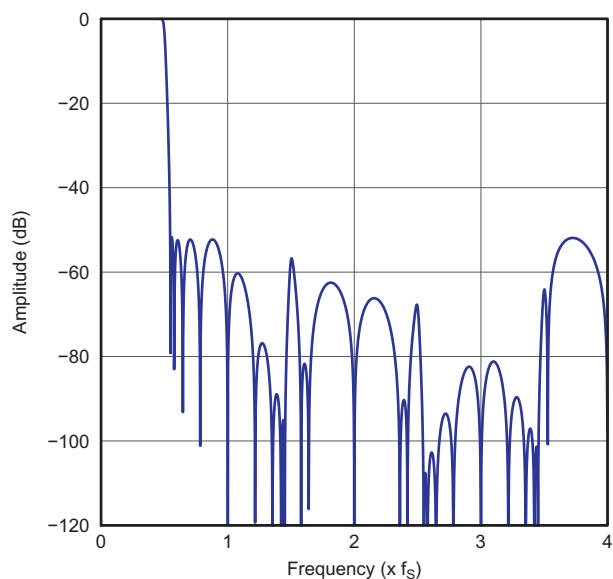


G028

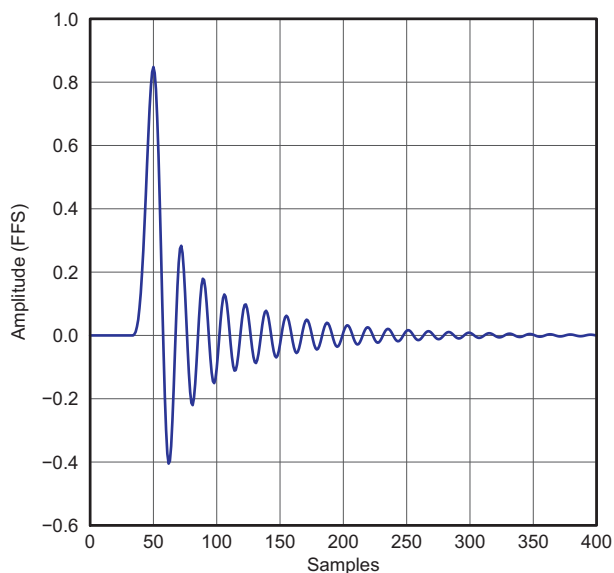
**Figure 43. Normal x2 Interpolation Filter Passband Ripple**

**Table 24. Low latency x8 Interpolation Filter, Single Rate**

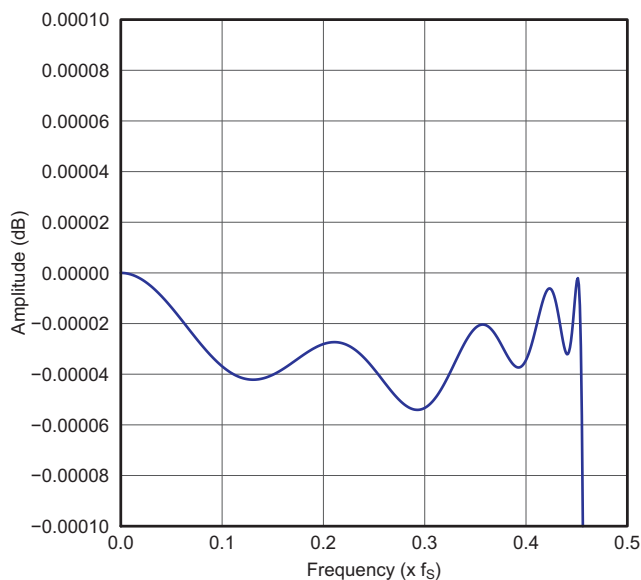
| Parameter             | Condition                                    | Value (Typical) | Value (Max) | Units |
|-----------------------|----------------------------------------------|-----------------|-------------|-------|
| Filter Gain Pass Band | 0 ..... 0.45f <sub>S</sub>                   |                 |             | dB    |
| Filter Gain Stop Band | 0.55f <sub>S</sub> ..... 7.455f <sub>S</sub> |                 |             | dB    |
| Filter Group Delay    |                                              |                 |             | S     |



G011

**Figure 44. Low latency x8 Interpolation Filter Frequency Response**

G022

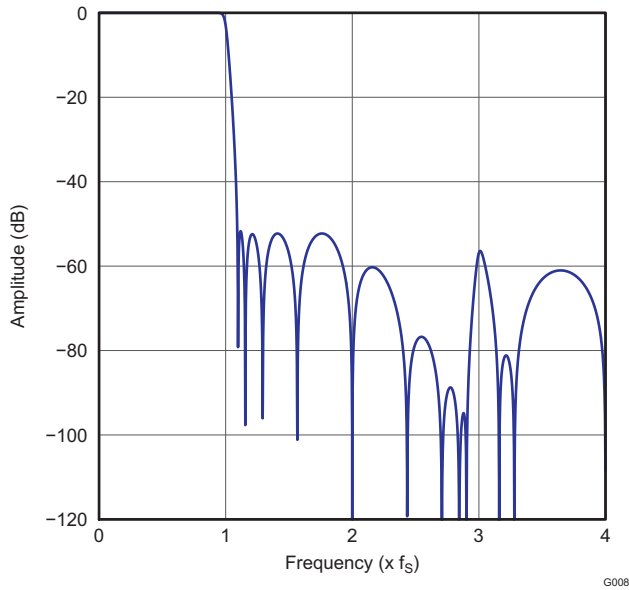
**Figure 45. Low latency x8 Interpolation Filter Impulse Response**

G033

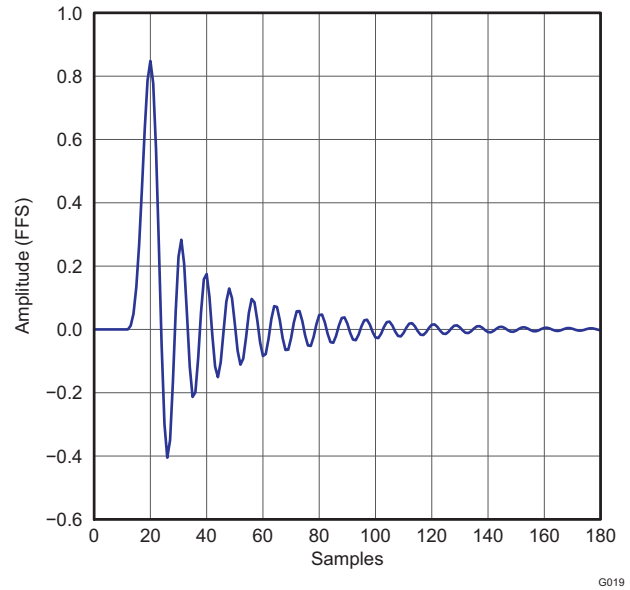
**Figure 46. Low latency x8 Interpolation Filter Passband Ripple**

**Table 25. Low latency x4 Interpolation Filter, Dual Rate**

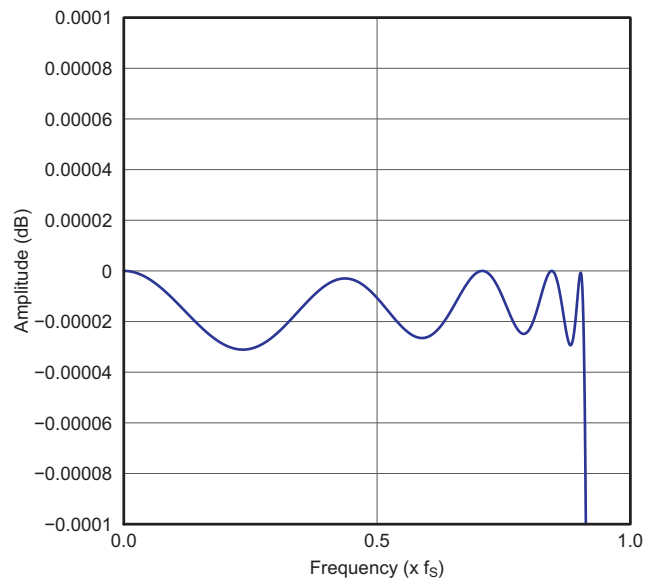
| Parameter             | Condition                                    | Value (Typical) | Value (Max) | Units |
|-----------------------|----------------------------------------------|-----------------|-------------|-------|
| Filter Gain Pass Band | 0 ..... 0.45f <sub>S</sub>                   |                 |             | dB    |
| Filter Gain Stop Band | 0.55f <sub>S</sub> ..... 3.455f <sub>S</sub> |                 |             | dB    |
| Filter Group Delay    |                                              |                 |             | S     |



**Figure 47. Low latency x4 Interpolation Filter Frequency Response**



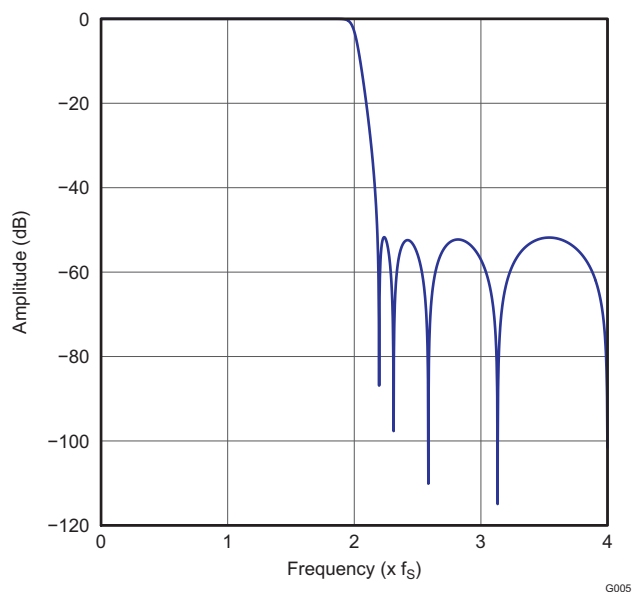
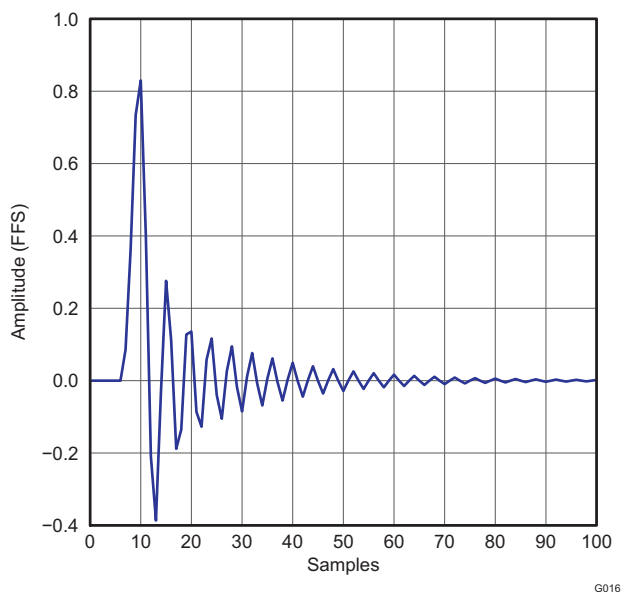
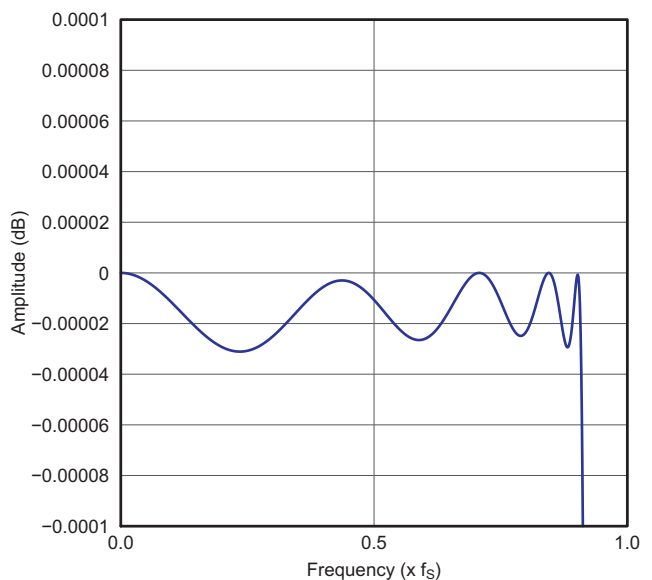
**Figure 48. Low latency x4 Interpolation Filter Impulse Response**



**Figure 49. Low latency x4 Interpolation Filter Passband Ripple**

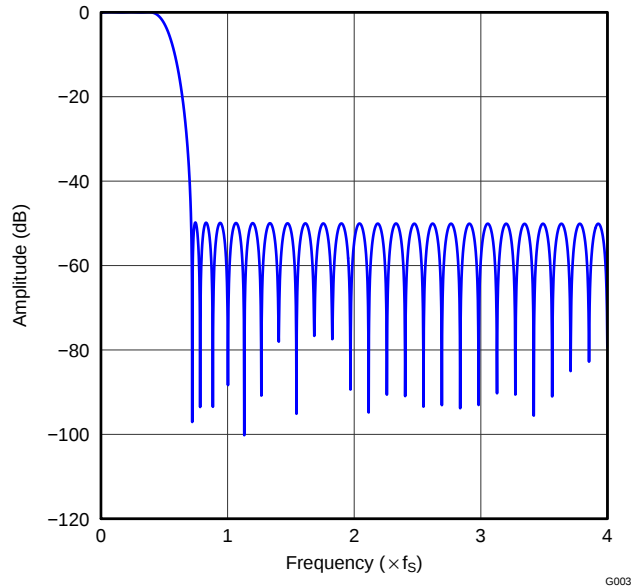
**Table 26. Low latency x2 Interpolation Filter, Quad Rate**

| Parameter             | Condition                                    | Value (Typical) | Value (Max) | Units |
|-----------------------|----------------------------------------------|-----------------|-------------|-------|
| Filter Gain Pass Band | 0 ..... 0.45f <sub>S</sub>                   |                 |             | dB    |
| Filter Gain Stop Band | 0.55f <sub>S</sub> ..... 1.455f <sub>S</sub> |                 |             | dB    |
| Filter Group Delay    |                                              |                 |             | S     |

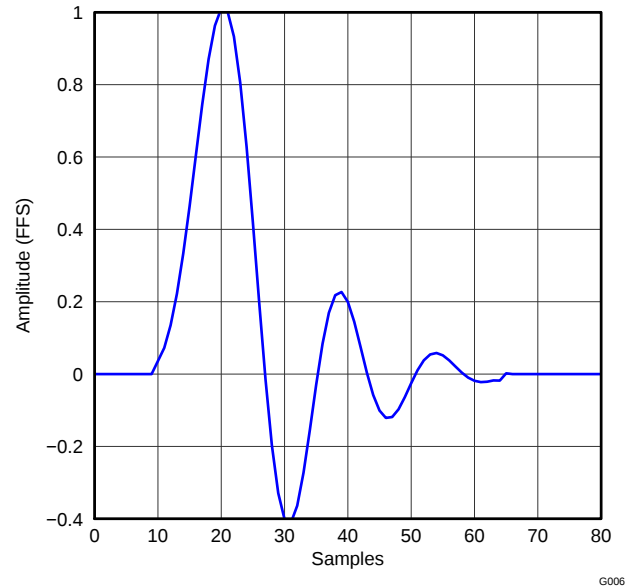
**Figure 50. Low latency x2 Interpolation Filter Frequency Response****Figure 51. Low latency x2 Interpolation Filter Impulse Response****Figure 52. Low latency x2 Interpolation Filter Passband Ripple**

**Table 27. Asymmetric FIR x8 Interpolation Filter, Single Rate**

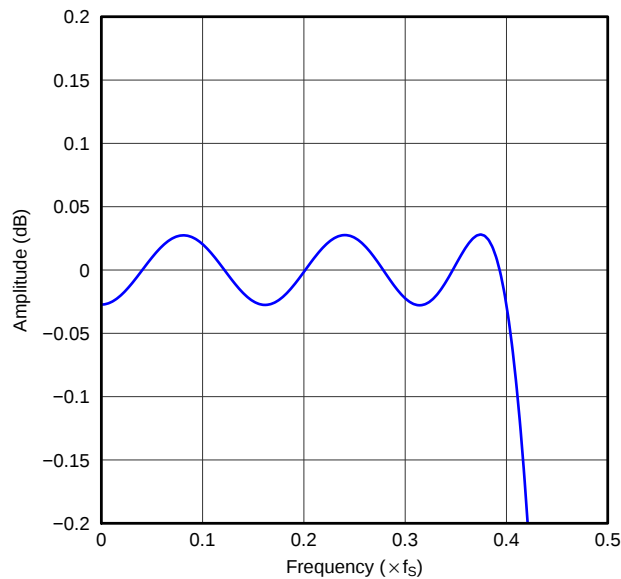
| Parameter             | Condition                                   | Value (Typical)   | Value (Max) | Units |
|-----------------------|---------------------------------------------|-------------------|-------------|-------|
| Filter Gain Pass Band | 0 ..... 0.40f <sub>S</sub>                  |                   | ±0.05       | dB    |
| Filter Gain Stop Band | 0.72f <sub>S</sub> ..... 7.28f <sub>S</sub> | –50               |             | dB    |
| Filter Group Delay    |                                             | 1.2t <sub>S</sub> |             | S     |



**Figure 53. Asymmetric FIR x8 Interpolation Filter Frequency Response, Single Rate**



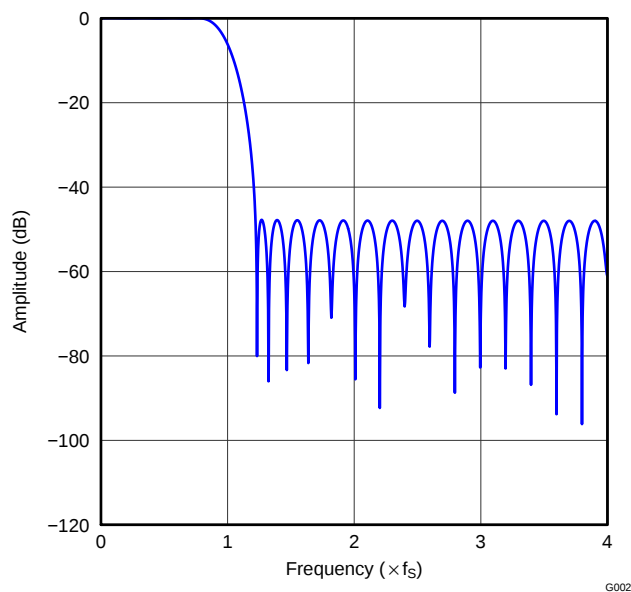
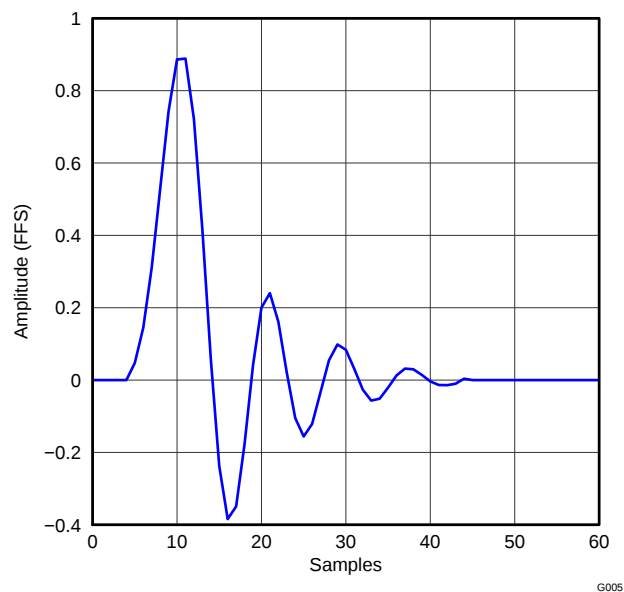
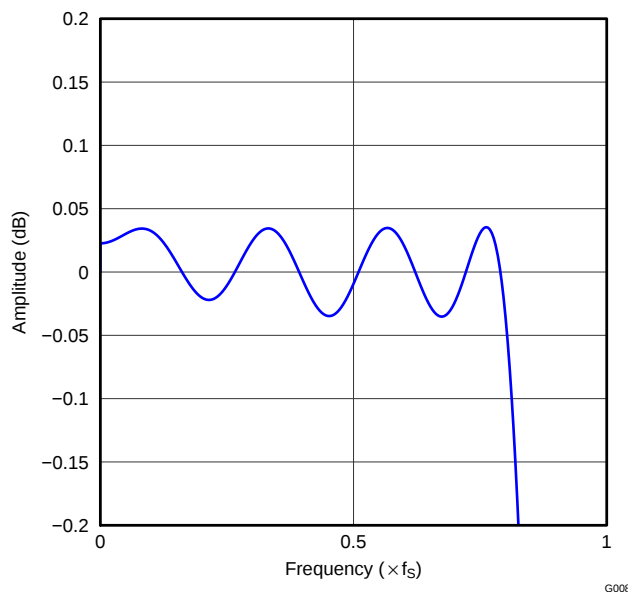
**Figure 54. Asymmetric FIR x8 Interpolation Filter Impulse Response, Single Rate**



**Figure 55. Asymmetric FIR x8 Interpolation Filter Passband Ripple, Single Rate**

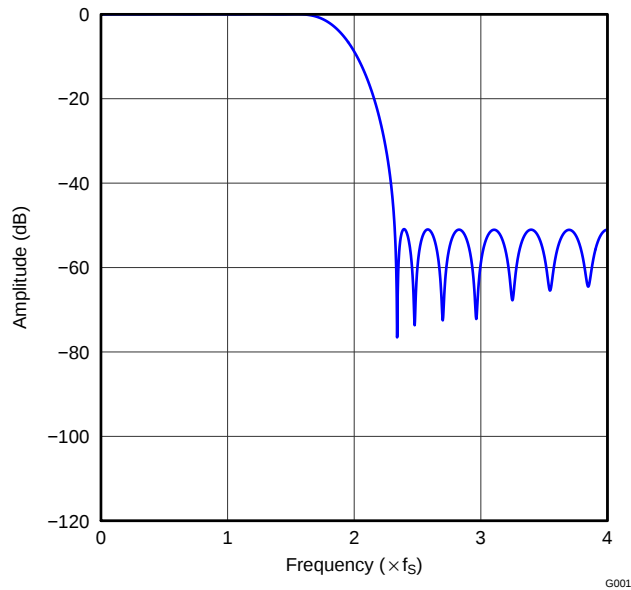
**Table 28. Asymmetric FIR x4 Interpolation Filter, Dual Rate**

| Parameter             | Condition                                   | Value (Typical)   | Value (Max) | Units |
|-----------------------|---------------------------------------------|-------------------|-------------|-------|
| Filter Gain Pass Band | 0 ..... 0.40f <sub>S</sub>                  |                   | ±0.05       | dB    |
| Filter Gain Stop Band | 0.72f <sub>S</sub> ..... 3.28f <sub>S</sub> | –50               |             | dB    |
| Filter Group Delay    |                                             | 1.2t <sub>S</sub> |             | S     |

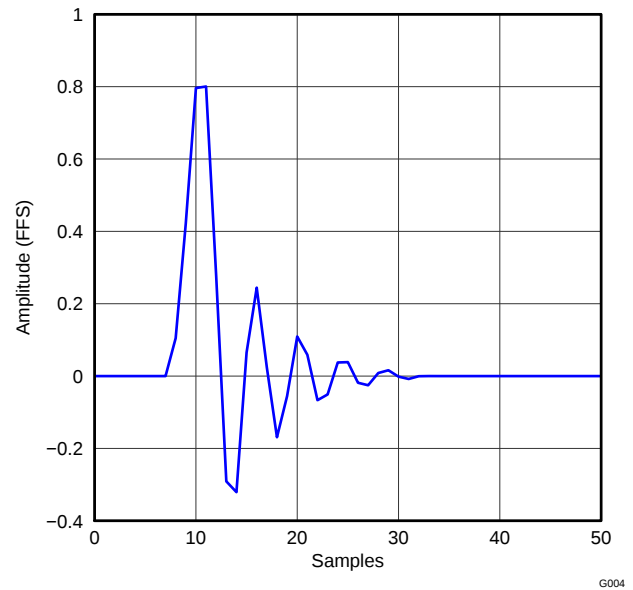
**Figure 56. Asymmetric FIR x4 Interpolation Filter Frequency Response, Dual Rate****Figure 57. Asymmetric FIR x4 Interpolation Filter Impulse Response, Dual Rate****Figure 58. Asymmetric x4 Interpolation Filter Passband Ripple, Dual Rate**

**Table 29. Asymmetric FIR x2 Interpolation Filter, Quad Rate**

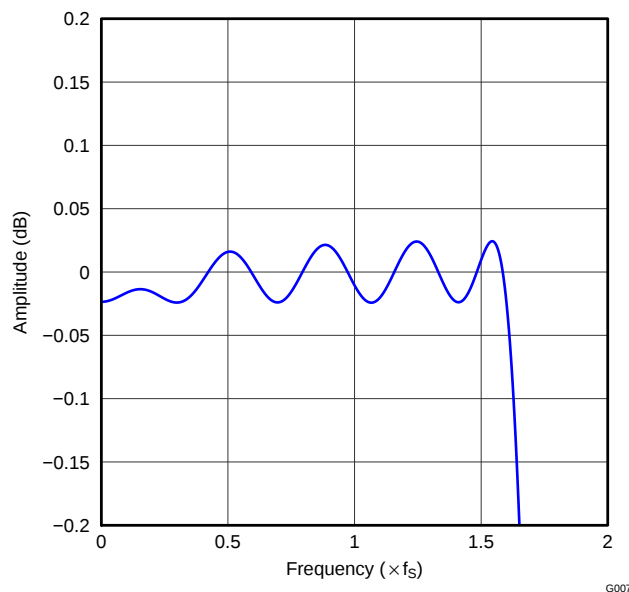
| Parameter             | Condition                                   | Value (Typical)   | Value (Max) | Units |
|-----------------------|---------------------------------------------|-------------------|-------------|-------|
| Filter Gain Pass Band | 0 ..... 0.40f <sub>S</sub>                  |                   | ±0.05       | dB    |
| Filter Gain Stop Band | 0.72f <sub>S</sub> ..... 1.28f <sub>S</sub> | –50               |             | dB    |
| Filter Group Delay    |                                             | 1.2t <sub>S</sub> |             | S     |



**Figure 59. Asymmetric FIR x2 Interpolation Filter Frequency Response, Quad Rate**



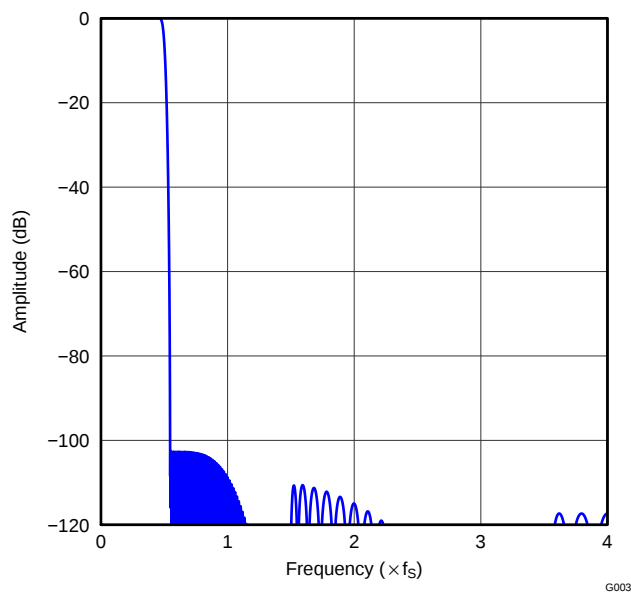
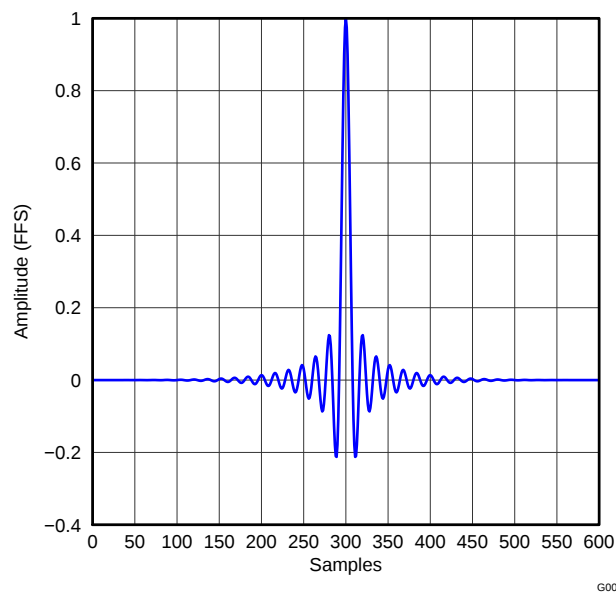
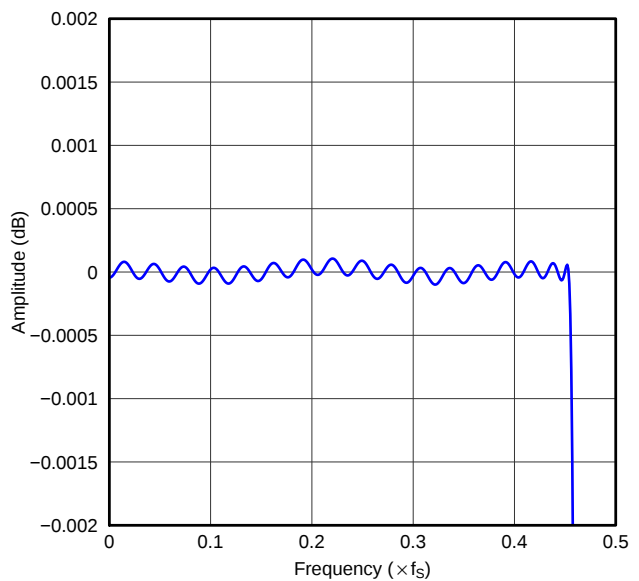
**Figure 60. Asymmetric FIR x2 Interpolation Filter Impulse Response, Quad Rate**



**Figure 61. Asymmetric x2 Interpolation Filter Passband Ripple, Quad Rate**

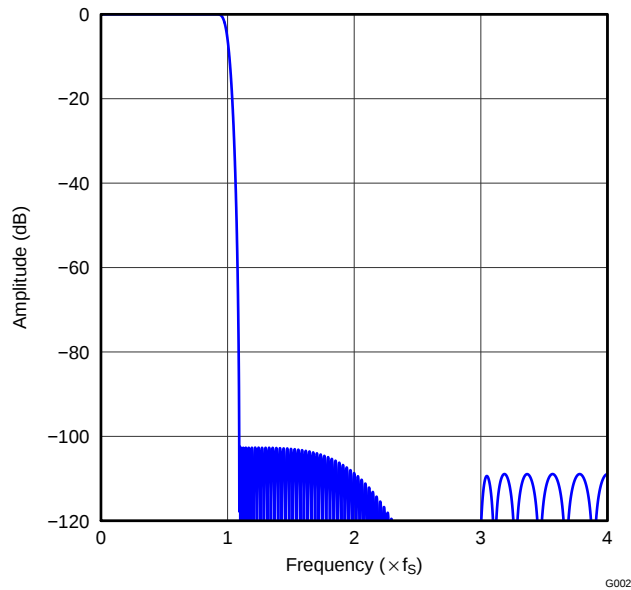
**Table 30. High-Attenuation x8 Interpolation Filter, Single Rate**

| Parameter             | Condition                  | Value (Typical) | Value (Max)  | Units |
|-----------------------|----------------------------|-----------------|--------------|-------|
| Filter Gain Pass Band | 0 ..... $0.45f_s$          |                 | $\pm 0.0005$ | dB    |
| Filter Gain Stop Band | $0.55f_s$ ..... $7.455f_s$ | -100            |              | dB    |
| Filter Group Delay    |                            | $33.7t_s$       |              | S     |

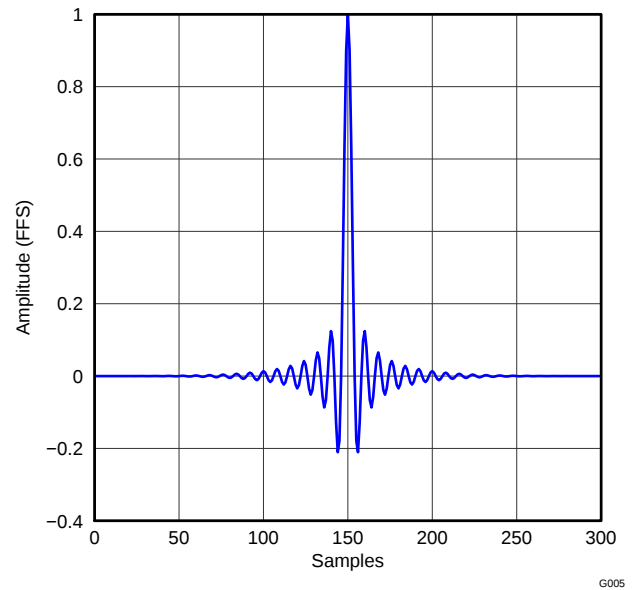
**Figure 62. High-Attenuation x8 Interpolation Filter Frequency Response, Single Rate****Figure 63. High-Attenuation x8 Interpolation Filter Impulse Response, Single Rate****Figure 64. High-Attenuation x8 Interpolation Filter Passband Ripple, Single Rate**

**Table 31. High-Attenuation x4 Interpolation Filter, Dual Rate**

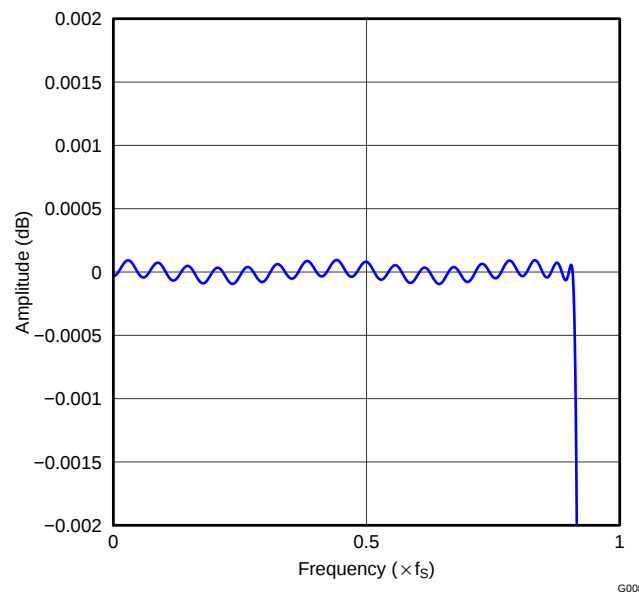
| Parameter             | Condition                  | Value (Typical) | Value (Max)  | Units |
|-----------------------|----------------------------|-----------------|--------------|-------|
| Filter Gain Pass Band | 0 ..... $0.45f_s$          |                 | $\pm 0.0005$ | dB    |
| Filter Gain Stop Band | $0.55f_s$ ..... $3.455f_s$ | -100            |              | dB    |
| Filter Group Delay    |                            | $33.7t_s$       |              | S     |



**Figure 65. High-Attenuation x4 Interpolation Filter Frequency Response, Dual Rate**



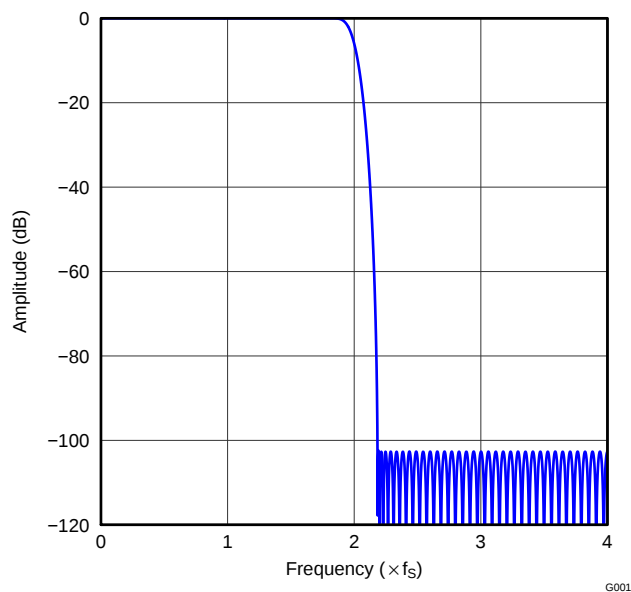
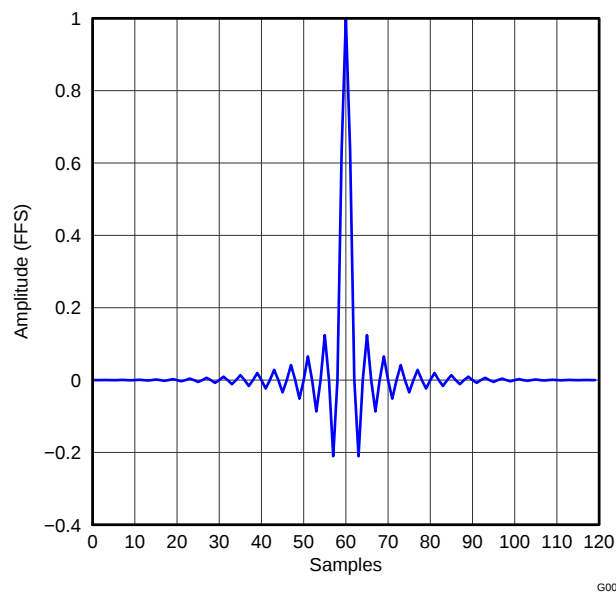
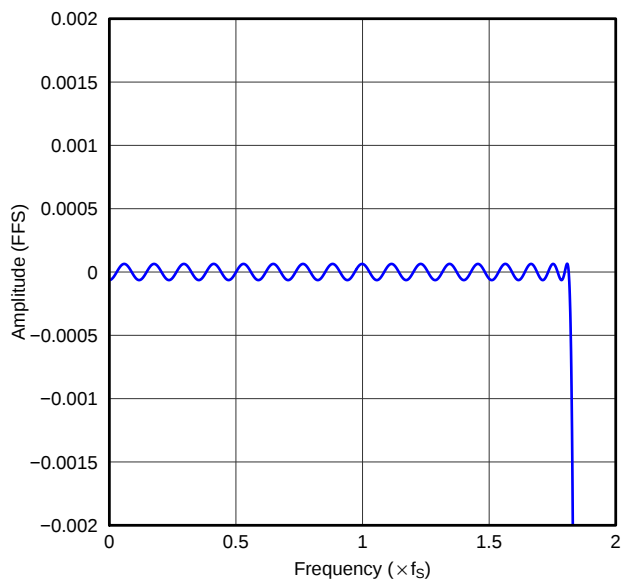
**Figure 66. High-Attenuation x4 Interpolation Filter Impulse Response, Dual Rate**



**Figure 67. High-Attenuation x4 Interpolation Filter Passband Ripple, Dual Rate**

**Table 32. High-Attenuation x2 Interpolation Filter, Quad Rate**

| Parameter             | Condition                  | Value (Typical) | Value (Max)  | Units |
|-----------------------|----------------------------|-----------------|--------------|-------|
| Filter Gain Pass Band | 0 ..... $0.45f_s$          |                 | $\pm 0.0005$ | dB    |
| Filter Gain Stop Band | $0.55f_s$ ..... $1.455f_s$ | -100            |              | dB    |
| Filter Group Delay    |                            | $33.7t_s$       |              | S     |

**Figure 68. High-Attenuation x2 Interpolation Filter Frequency Response, Quad Rate****Figure 69. High-Attenuation x2 Interpolation Filter Impulse Response, Quad Rate****Figure 70. High-Attenuation x2 Interpolation Filter Passband Ripple, Quad Rate**

## Fixed Audio Processing Flow (Program 5)

The PCM512x family implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The signal processing blocks available are:

- Biquad filters
- Multiband DRC
- Mono mixer
- Stereo mixer
- Average volume control

Users can find more details in Purepath Studio.

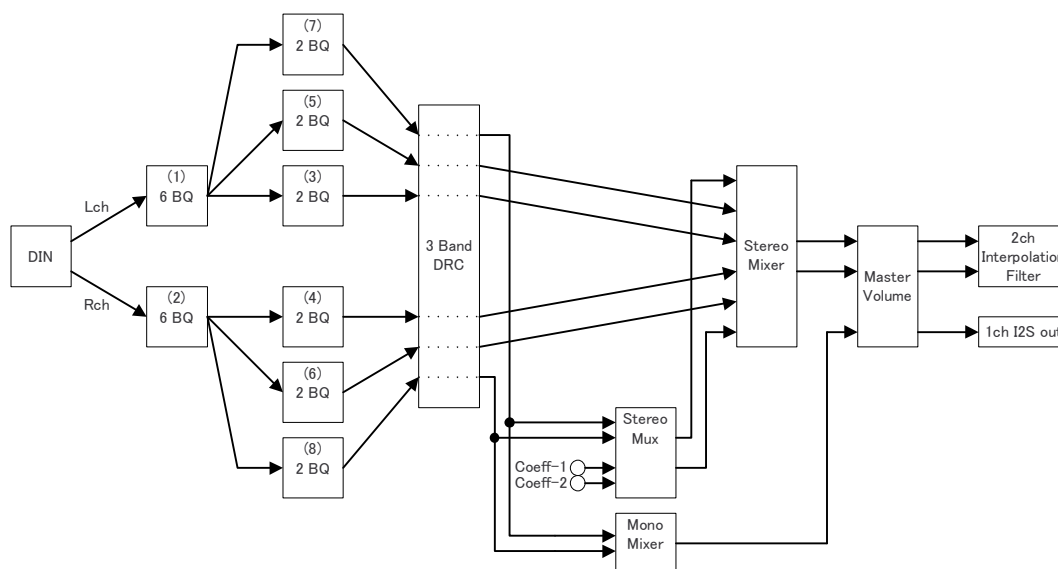
## Filter Programming Changes

The following sequence must be followed to change the ROM program.

1. Enter Stand-by mode. (Set Page 0, Register 2, D(4))
2. Change program number. (Set Page 0, Register 43, D(4:0))
3. Exit Stand-by mode. (Reset Page.0, Register 2, D(4))

## Processing Blocks – Detailed Descriptions

Figure 71 shows the fixed processing flow.



**Figure 71. Preset Process Flow**

Figure 72 shows a screen capture of PurePath Studio.

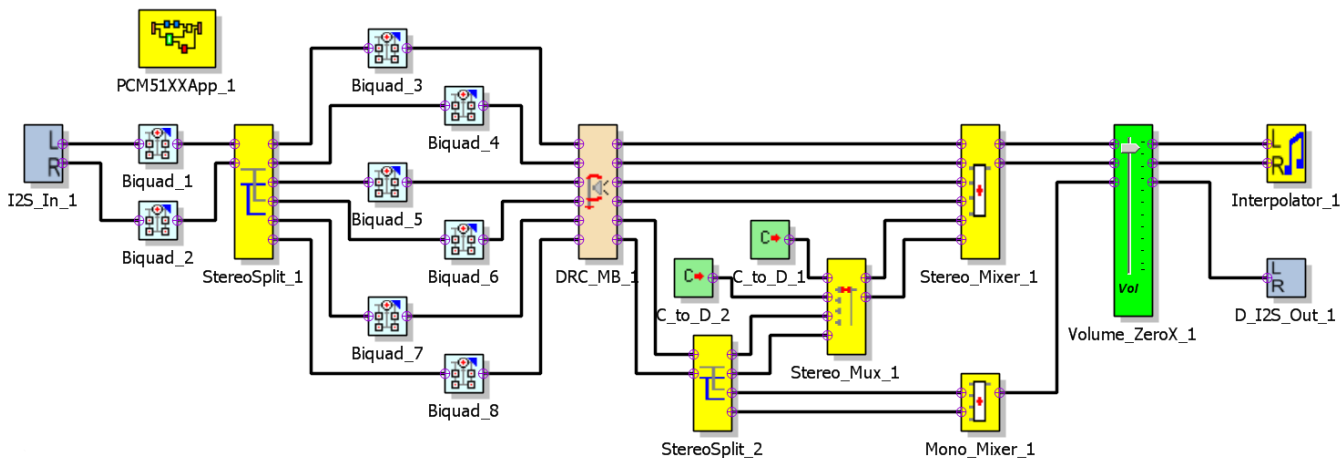


Figure 72. PurePath Studio Screen Capture

**Biquad Section**

The transfer function of each of the biquad filters is given by

$$H(z) = \frac{N_0 + 2N_1z^{-1} + N_2z^{-2}}{2^{23} - 2D_1z^{-1} - D_2z^{-2}} \tag{2}$$

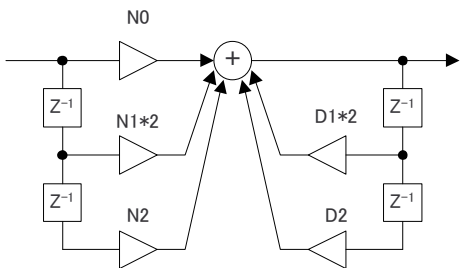


Figure 73. Biquad Block

Table 33. Biquad Filter Coefficients

| Filter                        | Channel     | Coefficient | Register                     |
|-------------------------------|-------------|-------------|------------------------------|
| BIQUAD (1) - 1 BIQUAD (2) - 1 | Lch,<br>Rch | N0          | C10 (Pg 44, Reg 48,49,50,51) |
|                               |             | N1          | C11 (Pg 44, Reg 52,53,54,55) |
|                               |             | N2          | C12 (Pg 44, Reg 56,57,58,59) |
|                               |             | D1          | C13 (Pg 44, Reg 60,61,62,63) |
|                               |             | D2          | C14 (Pg 44, Reg 64,65,66,67) |
| BIQUAD (1) - 2 BIQUAD (2) - 2 | Lch,<br>Rch | N0          | C15 (Pg 44, Reg 68,69,70,71) |
|                               |             | N1          | C16 (Pg 44, Reg 72,73,74,75) |
|                               |             | N2          | C17 (Pg 44, Reg 76,77,78,79) |
|                               |             | D1          | C18 (Pg 44, Reg 80,81,82,83) |
|                               |             | D2          | C19 (Pg 44, Reg 84,85,86,87) |

**Table 33. Biquad Filter Coefficients (continued)**

| Filter                        | Channel     | Coefficient | Register                            |
|-------------------------------|-------------|-------------|-------------------------------------|
| BIQUAD (1) - 3 BIQUAD (2) - 3 | Lch,<br>Rch | N0          | C20 (Pg 44, Reg 88,89,90,91)        |
|                               |             | N1          | C21 (Pg 44, Reg 92,93,94,95)        |
|                               |             | N2          | C22 (Pg 44, Reg 96,97,98,99)        |
|                               |             | D1          | C23 (Pg 44, Reg 100,101, 102, 103)  |
|                               |             | D2          | C24 (Pg 44, Reg 104, 105, 106, 107) |
| BIQUAD (1) - 4 BIQUAD (2) - 4 | Lch,<br>Rch | N0          | C25 (Pg 44, Reg 108, 109, 110, 111) |
|                               |             | N1          | C26 (Pg 44, Reg 112, 113, 114, 115) |
|                               |             | N2          | C27 (Pg 44, Reg 116, 117, 118, 119) |
|                               |             | D1          | C28 (Pg 44, Reg 120, 121, 122, 123) |
|                               |             | D2          | C29 (Pg 44, Reg 124, 125, 126, 127) |
| BIQUAD (1) - 5 BIQUAD (2) - 5 | Lch,<br>Rch | N0          | C30 (Pg 45, Reg 8, 9, 10, 11)       |
|                               |             | N1          | C31 (Pg 45, Reg 12, 13, 14, 15)     |
|                               |             | N2          | C32 (Pg 45, Reg 16, 17, 18, 19)     |
|                               |             | D1          | C33 (Pg 45, Reg 20, 21, 22, 23)     |
|                               |             | D2          | C34 (Pg 45, Reg 24, 25, 26, 27)     |
| BIQUAD (1) - 6 BIQUAD (2) - 6 | Lch,<br>Rch | N0          | C35 (Pg 45, Reg 28, 29, 30, 31)     |
|                               |             | N1          | C36 (Pg 45, Reg 32, 33, 34, 35)     |
|                               |             | N2          | C37 (Pg 45, Reg 36, 37, 38, 39)     |
|                               |             | D1          | C38 (Pg 45, Reg 40, 41, 42, 43)     |
|                               |             | D2          | C39 (Pg 45, Reg 44, 45, 46, 47)     |
| BIQUAD (3) - 1 BIQUAD (4) - 1 | Lch,<br>Rch | N0          | C40 (Pg 45, Reg 48, 49, 50, 51)     |
|                               |             | N1          | C41 (Pg 45, Reg 52, 53, 54, 55)     |
|                               |             | N2          | C42 (Pg 45, Reg 56, 57, 58, 59)     |
|                               |             | D1          | C43 (Pg 45, Reg 60, 61, 62, 63)     |
|                               |             | D2          | C44 (Pg 45, Reg 64, 65, 66, 67)     |
| BIQUAD (3) - 2 BIQUAD (4) - 2 | Lch,<br>Rch | N0          | C45 (Pg 45, Reg 68, 69, 70, 71)     |
|                               |             | N1          | C46 (Pg 45, Reg 72, 73, 74, 75)     |
|                               |             | N2          | C47 (Pg 45, Reg 76, 77, 78, 79)     |
|                               |             | D1          | C48 (Pg 45, Reg 80, 81, 82, 83)     |
|                               |             | D2          | C49 (Pg 45, Reg 84, 85, 86, 87)     |
| BIQUAD (5) - 1 BIQUAD (6) - 1 | Lch,<br>Rch | N0          | C50 (Pg 45, Reg 88, 89, 90, 91)     |
|                               |             | N1          | C51 (Pg 45, Reg 92, 93, 94, 95)     |
|                               |             | N2          | C52 (Pg 45, Reg 96, 97, 98, 99)     |
|                               |             | D1          | C53 (Pg 45, Reg 100, 101, 102, 103) |
|                               |             | D2          | C54 (Pg 45, Reg 104, 105, 106, 107) |
| BIQUAD (5) - 2 BIQUAD (6) - 2 | Lch,<br>Rch | N0          | C55 (Pg 45, Reg 108, 109, 110, 111) |
|                               |             | N1          | C56 (Pg 45, Reg 112, 113, 114, 115) |
|                               |             | N2          | C57 (Pg 45, Reg 116, 117, 118, 119) |
|                               |             | D1          | C58 (Pg 45, Reg 120, 121, 122, 123) |
|                               |             | D2          | C59 (Pg 45, Reg 124, 125, 126, 127) |
| BIQUAD (7) - 1 BIQUAD (8) - 1 | Lch,<br>Rch | N0          | C60 (Pg 46, Reg 8, 9, 10, 11)       |
|                               |             | N1          | C61 (Pg 46, Reg 12, 13, 14, 15)     |
|                               |             | N2          | C62 (Pg 46, Reg 16, 17, 18, 19)     |
|                               |             | D1          | C63 (Pg 46, Reg 20, 21, 22, 23)     |
|                               |             | D2          | C64 (Pg 46, Reg 24, 25, 26, 27)     |

**Table 33. Biquad Filter Coefficients (continued)**

| Filter                        | Channel     | Coefficient | Register                        |
|-------------------------------|-------------|-------------|---------------------------------|
| BIQUAD (7) - 2 BIQUAD (8) - 2 | Lch,<br>Rch | N0          | C65 (Pg 46, Reg 28, 29, 30, 31) |
|                               |             | N1          | C66 (Pg 46, Reg 32, 33, 34, 35) |
|                               |             | N2          | C67 (Pg 46, Reg 36, 37, 38, 39) |
|                               |             | D1          | C68 (Pg 46, Reg 40, 41, 42, 43) |
|                               |             | D2          | C69 (Pg 46, Reg 44, 45, 46, 47) |

## Dynamic Range Compression

Dynamic range compression (DRC) improves the overall listening experience. Typical music signals are characterized by crest factors (the ratio of peak signal power to average signal power) of 12dB or more. To avoid audible distortion due to clipping of peak signals, the gain of the DAC channel must be adjusted so as not to cause hard clipping. As a result, the low applied gain during nominal periods causes the perception that the signal is not loud enough. To overcome this problem, the DRC in the PCM512x continuously monitors the output of the DAC Digital Volume control to detect its power level with respect to 0dB full-scale. When the power level is low, the DRC increases the input signal gain to make it sound louder, and reduces the gain during peaks to avoid hard clipping. The DRC enables louder audio during nominal periods with a clearer, more pleasant listening experience.

The 3-band DRC function applies DRC to 3 different mono/stereo signals with 3 different time constants. The same DRC curve is applied on all the signals, enabling a multi-band DRC solution. The underlying DRC algorithm is the same as that available with the DRC component in PurePath Studio. In this instance, the DRC gain acts on each signal in time-multiplexed order, for example, 1-2-3, 1-2-3, 1-2-3.

**Table 34. DRC Coefficients**

| Coefficient           | Register                            | Description |
|-----------------------|-------------------------------------|-------------|
| DRC_MB_1_DRC_1_DRCAE  | C70 (Pg 46, Reg 48, 49, 50, 51)     |             |
| DRC_MB_1_DRC_1_DRC1AE | C71 (Pg 46, Reg 52, 53, 54, 55)     |             |
| DRC_MB_1_DRC_1_DRCAA  | C72 (Pg 46, Reg 56, 57, 58, 59)     |             |
| DRC_MB_1_DRC_1_DRC1AA | C73 (Pg 46, Reg 60, 61, 62, 63)     |             |
| DRC_MB_1_DRC_1_DRCAD  | C74 (Pg 46, Reg 64, 65, 66, 67)     |             |
| DRC_MB_1_DRC_1_DRC1AD | C75 (Pg 46, Reg 68, 69, 70, 71)     |             |
| DRC_MB_1_DRC_2_DRCAE  | C76 (Pg 46, Reg 72, 73, 74, 75)     |             |
| DRC_MB_1_DRC_2_DRC1AE | C77 (Pg 46, Reg 76, 77, 78, 79)     |             |
| DRC_MB_1_DRC_2_DRCAA  | C78 (Pg 46, Reg 80, 81, 82, 83)     |             |
| DRC_MB_1_DRC_2_DRC1AA | C79 (Pg 46, Reg 84, 85, 86, 87)     |             |
| DRC_MB_1_DRC_2_DRCAD  | C80 (Pg 46, Reg 88, 89, 90, 91)     |             |
| DRC_MB_1_DRC_2_DRC1AD | C81 (Pg 46, Reg 92, 93, 94, 95)     |             |
| DRC_MB_1_DRC_3_DRCAE  | C82 (Pg 46, Reg 96, 97, 98, 99)     |             |
| DRC_MB_1_DRC_3_DRC1AE | C83 (Pg 46, Reg 100, 101, 102, 103) |             |
| DRC_MB_1_DRC_3_DRCAA  | C84 (Pg 46, Reg 104, 105, 106, 107) |             |
| DRC_MB_1_DRC_3_DRC1AA | C85 (Pg 46, Reg 108, 109, 110, 111) |             |
| DRC_MB_1_DRC_3_DRCAD  | C86 (Pg 46, Reg 112, 113, 114, 115) |             |
| DRC_MB_1_DRC_3_DRC1AD | C87 (Pg 46, Reg 116, 117, 118, 119) |             |
| DRC_MB_1_DRC_DRCK0    | C88 (Pg 46, Reg 120, 121, 122, 123) |             |
| DRC_MB_1_DRC_DRCK1    | C89 (Pg 46, Reg 124, 125, 126, 127) |             |
| DRC_MB_1_DRC_DRCK2    | C90 (Pg 47, Reg 8, 9, 10, 11)       |             |
| DRC_MB_1_DRC_DRCMT1   | C91 (Pg 47, Reg 12, 13, 14, 15)     |             |
| DRC_MB_1_DRC_DRCMT2   | C92 (Pg 47, Reg 16, 17, 18, 19)     |             |
| DRC_MB_1_DRC_DRCOFF1  | C93 (Pg 47, Reg 20, 21, 22, 23)     |             |
| DRC_MB_1_DRC_DRCOFF2  | C94 (Pg 47, Reg 24, 25, 26, 27)     |             |
| DRC_MB_1_MinusOne_Q22 | C95 (Pg 47, Reg 28, 29, 30, 31)     |             |

**Table 34. DRC Coefficients (continued)**

| <b>Coefficient</b>        | <b>Register</b>                      | <b>Description</b> |
|---------------------------|--------------------------------------|--------------------|
| DRC_MB_1_MinusTwo_Q22     | C96 (Pg 47, Reg 32, 33, 34, 35)      |                    |
| DRC_MB_1_One_M2           | C97 (Pg 47, Reg 36, 37, 38, 39)      |                    |
| DRC_MB_1_Zero             | C98 (Pg 47, Reg 40, 41, 42, 43)      |                    |
| DRC_MB_1_En_dB            | C99 (Pg 47, Reg 44, 45, 46, 47)      |                    |
| DRC_MB_1_Minus_Zero_dB    | C100 (Pg 47, Reg 48, 49, 50, 51)     |                    |
| DRC_MB_1_60_dB            | C101 (Pg 47, Reg 52, 53, 54, 55)     |                    |
| DRC_MB_1_Minus_60_dB      | C102 (Pg 47, Reg 56, 57, 58, 59)     |                    |
| DRC_MB_1_12_dB            | C103 (Pg 47, Reg 60, 61, 62, 63)     |                    |
| DRC_MB_1_Offset           | C104 (Pg 47, Reg 64, 65, 66, 67)     |                    |
| DRC_MB_1_K                | C105 (Pg 47, Reg 68, 69, 70, 71)     |                    |
| DRC_MB_1_x / DRC_MB_1_DRC | C106 (Pg 47, Reg 72, 73, 74, 75)     |                    |
| DRC_MB_1_48_dB            | C107 (Pg 47, Reg 76, 77, 78, 79)     |                    |
| DRC_MB_1_Minus_48_dB      | C108 (Pg 47, Reg 80, 81, 82, 83)     |                    |
| DRC_MB_1_c1_3             | C109 (Pg 47, Reg 84, 85, 86, 87)     |                    |
| DRC_MB_1_c1_2             | C110 (Pg 47, Reg 88, 89, 90, 91)     |                    |
| DRC_MB_1_c1_1             | C111 (Pg 47, Reg 92, 93, 94, 95)     |                    |
| DRC_MB_1_c1_0             | C112 (Pg 47, Reg 96, 97, 98, 99)     |                    |
| DRC_MB_1_O1_1             | C113 (Pg 47, Reg 100, 101, 102, 103) |                    |
| DRC_MB_1_S1_1             | C114 (Pg 47, Reg 104, 105, 106, 107) |                    |
| DRC_MB_1_O1_2             | C115 (Pg 47, Reg 108, 109, 110, 111) |                    |
| DRC_MB_1_S1_2             | C116 (Pg 47, Reg 112, 113, 114, 115) |                    |
| DRC_MB_1_O1_3             | C117 (Pg 47, Reg 116, 117, 118, 119) |                    |
| DRC_MB_1_S1_3             | C118 (Pg 47, Reg 120, 121, 122, 123) |                    |
| DRC_MB_1_One_1_Q17        | C119 (Pg 47, Reg 124, 125, 126, 127) |                    |
| DRC_MB_1_Scale1           | C120 (Pg 48, Reg 8, 9, 10, 11)       |                    |
| DRC_MB_1_x1Coeff          | C121 (Pg 48, Reg 12, 13, 14, 15)     |                    |
| DRC_MB_1_c2_3             | C122 (Pg 48, Reg 16, 17, 18, 19)     |                    |
| DRC_MB_1_c2_2             | C123 (Pg 48, Reg 20, 21, 22, 23)     |                    |
| DRC_MB_1_c2_1             | C124 (Pg 48, Reg 24, 25, 26, 27)     |                    |
| DRC_MB_1_c2_0             | C125 (Pg 48, Reg 28, 29, 30, 31)     |                    |
| DRC_MB_1_O2_1             | C126 (Pg 48, Reg 32, 33, 34, 35)     |                    |
| DRC_MB_1_S2_1             | C127 (Pg 48, Reg 36, 37, 38, 39)     |                    |
| DRC_MB_1_O2_2             | C128 (Pg 48, Reg 40, 41, 42, 43)     |                    |
| DRC_MB_1_S2_2             | C129 (Pg 48, Reg 44, 45, 46, 47)     |                    |
| DRC_MB_1_O2_3             | C130 (Pg 48, Reg 48, 49, 50, 51)     |                    |
| DRC_MB_1_S2_3             | C131 (Pg 48, Reg 52, 53, 54, 55)     |                    |
| DRC_MB_1_One_2_Q17        | C132 (Pg 48, Reg 56, 57, 58, 59)     |                    |
| DRC_MB_1_Scale2           | C133 (Pg 48, Reg 60, 61, 62, 63)     |                    |
| DRC_MB_1_x2Coeff          | C134 (Pg 48, Reg 64, 65, 66, 67)     |                    |
| DRC_MB_1_R1_1             | C135 (Pg 48, Reg 68, 69, 70, 71)     |                    |
| DRC_MB_1_R1_2             | C136 (Pg 48, Reg 72, 73, 74, 75)     |                    |
| DRC_MB_1_R2_1             | C137 (Pg 48, Reg 76, 77, 78, 79)     |                    |
| DRC_MB_1_R2_2             | C138 (Pg 48, Reg 80, 81, 82, 83)     |                    |
| DRC_MB_1_Band1_GainC      | C139 (Pg 48, Reg 84, 85, 86, 87)     |                    |
| DRC_MB_1_Band2_GainC      | C140 (Pg 48, Reg 88, 89, 90, 91)     |                    |
| DRC_MB_1_Band3_GainC      | C141 (Pg 48, Reg 92, 93, 94, 95)     |                    |
| DRC_MB_1_MinusOne_M1      | C142 (Pg 48, Reg 96, 97, 98, 99)     |                    |

**Table 34. DRC Coefficients (continued)**

| Coefficient           | Register                             | Description |
|-----------------------|--------------------------------------|-------------|
| DRC_MB_1_One_M1       | C143 (Pg 48, Reg 100, 101, 102, 103) |             |
| DRC_MB_1_Band1_GainE  | C144 (Pg 48, Reg 104, 105, 106, 107) |             |
| DRC_MB_1_Band2_GainE  | C145 (Pg 48, Reg 108, 109, 110, 111) |             |
| DRC_MB_1_Band3_GainE  | C146 (Pg 48, Reg 112, 113, 114, 115) |             |
| DRC_MB_1_minus_One_M2 | C147 (Pg 48, Reg 116, 117, 118, 119) |             |

## Stereo Mixer

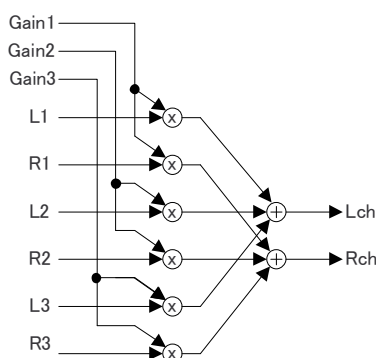
Three stereo inputs are mixed into one stereo output with input signal gain given by [Equation 3](#).

$$\text{Out\_L}(n) = \sum (\text{Input\_L}(i,n) \cdot \text{Gain}(i))$$

where

- $i=1:2,3$  (3)

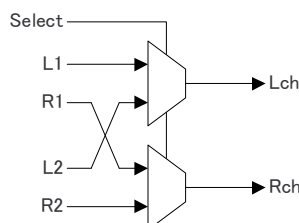
[Figure 74](#) and [Table 35](#) show the stereo mixer operation.

**Figure 74. Figure 4. Stereo Mixer Block****Table 35. Stereo Mixer Coefficients**

| Coefficient             | Register                             | Description |
|-------------------------|--------------------------------------|-------------|
| Stereo_Mixer_1_MixGain1 | C148 (Pg 48, Reg 120, 121, 122, 123) |             |
| Stereo_Mixer_1_MixGain2 | C149 (Pg 48, Reg 124, 125, 126, 127) |             |
| Stereo_Mixer_1_MixGain3 | C150 (Pg 49, Reg 8, 9, 10, 11)       |             |

## Stereo Multiplexer

The Stereo Multiplexer selects one or 2 from 4 stereo input channels.

**Figure 75. Stereo Multiplexer Block**

**Table 36. Stereo Multiplexer Select Coefficient**

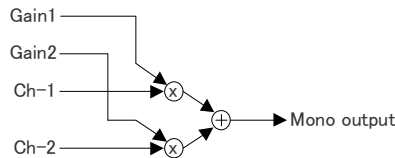
| Coefficient            | Register                         | Description |
|------------------------|----------------------------------|-------------|
| Stereo_Mux_1_MuxSelect | C152 (Pg 49, Reg 16, 17, 18, 19) |             |

**Table 37. Stereo Multiplexer Input Coefficient**

| Coefficient                          | Register                         | Description |
|--------------------------------------|----------------------------------|-------------|
| C_to_D_1_Coefval<br>C_to_D_2_Coefval | C153 (Pg 49, Reg 20, 21, 22, 23) |             |

## Mono Mixer

The Mono Mixer computes a weighted sum of 2 input channels and produces an output.


**Figure 76. Figure 6. Mono Mixer Block**
**Table 38. Mono Mixer Coefficients**

| Coefficient           | Register                         | Description |
|-----------------------|----------------------------------|-------------|
| Mono_Mixer_1_MixGain1 | C154 (Pg 49, Reg 24, 25, 26, 27) |             |
| Mono_Mixer_1_MixGain2 | C155 (Pg 49, Reg 28, 29, 30, 31) |             |

## Master Volume Control

The Master Volume controls the volume using a linear ramp and zero crossing detection for transitions.

**Table 39. Mono Mixer Coefficients**

| Coefficient                          | Register                             | Description |
|--------------------------------------|--------------------------------------|-------------|
| Volume_ZeroX_1_volcmd                | C158 (Pg 49, Reg 40, 41, 42, 43)     |             |
| Volume_ZeroX_1_volout                | C159 (Pg 49, Reg 44, 45, 46, 47)     |             |
| Volume_ZeroX_1_volout_loudness       | C160 (Pg 49, Reg 48, 49, 50, 51)     |             |
| Volume_ZeroX_1_MinusOne_M2           | C161 (Pg 49, Reg 52, 53, 54, 55)     |             |
| Volume_ZeroX_1_workingval_1_pre_CRAM | C162 (Pg 49, Reg 56, 57, 58, 59)     |             |
| Volume_ZeroX_1_volout_pre1           | C163 (Pg 49, Reg 60, 61, 62, 63)     |             |
| Volume_ZeroX_1_workingval_2_pre_CRAM | C164 (Pg 49, Reg 64, 65, 66, 67)     |             |
| Volume_ZeroX_1_volout_pre2           | C165 (Pg 49, Reg 68, 69, 70, 71)     |             |
| Volume_ZeroX_1_workingval_3_pre_CRAM | C166 (Pg 49, Reg 72, 73, 74, 75)     |             |
| Volume_ZeroX_1_volout_pre3           | C167 (Pg 49, Reg 76, 77, 78, 79)     |             |
| Volume_ZeroX_1_One_M2                | C168 (Pg 49, Reg 80, 81, 82, 83)     |             |
| Volume_ZeroX_1_Zero                  | C169 (Pg 49, Reg 84, 85, 86, 87)     |             |
| MinusOne_Int                         | C170 (Pg 49, Reg 88, 89, 90, 91)     |             |
| MinusOne_M1                          | C171 (Pg 49, Reg 92, 93, 94, 95)     |             |
| One_M2                               | C172 (Pg 49, Reg 96, 97, 98, 99)     |             |
| One_M1                               | C173 (Pg 49, Reg 100, 101, 102, 103) |             |
| Zero                                 | C174 (Pg 49, Reg 104, 105, 106, 107) |             |

## Miscellaneous Coefficients

**Table 40. Miscellaneous Coefficients**

| Coefficient               | Register                             | Description |
|---------------------------|--------------------------------------|-------------|
| DRC_MB_1_DataBlock        | C175 (Pg 49, Reg 108, 109, 110, 111) |             |
| DRC_MB_1_CoeffBlock       | C176 (Pg 49, Reg 112, 113, 114, 115) |             |
| Volume_ZeroX_1_DataBlock  | C177 (Pg 49, Reg 116, 117, 118, 119) |             |
| Volume_ZeroX_1_CoeffBlock | C178 (Pg 49, Reg 120, 121, 122, 123) |             |
| plus_one                  | C179 (Pg 49, Reg 124, 125, 126, 127) |             |
| ADD_OF_filter_in_L        | C180 (Pg 50, Reg 8, 9, 10, 11)       |             |
| ADD_OF_filter_in_R        | C181 (Pg 50, Reg 12, 13, 14, 15)     |             |

## Analog Gain Control

Analog gain control can be selected between  $2V_{rms}$  FS (0dB) or  $1V_{rms}$  FS (-6dB). Gain is controlled via hardware by the AGNS pin, and via software (SPI/I<sup>2</sup>C), Page 1, Register 2, D4(L-ch) / D0(R-ch).

## Digital Volume Control

A basic digital volume control with range from 24 dB to -103 dB and mute is available on each channels by Page 0, Register 61, D(7:0) for L-ch and Register 62, D(7:0) for R-ch. These volume controls all have 0.5 dB step programmability over most gain and attenuation ranges. [Table 41](#) lists the detailed gain versus programmed setting for this basic volume control. Volume can be changed for both L-ch and R-ch at the same time or independently by Page 0, Register 60, D(1:0). When D(1:0) set 00 (default), independent control is selected. When D(1:0) set 01, R-ch accords with L-ch volume. When D(1:0) set 10, L-ch accords with R-ch volume. To set D(1:0) to 11 is prohibited.

**Table 41. Digital Volume Control Settings**

| Gain Setting | Binary Data | Gain (dB) | Comments                 |
|--------------|-------------|-----------|--------------------------|
| 0            | 0000-0000   | 24.0      | Positive maximum         |
| 1            | 0000-0001   | 23.5      |                          |
| :            | :           | :         |                          |
| 46           | 0010-1110   | 1.0       |                          |
| 47           | 0010-1111   | 0.5       |                          |
| 48           | 0011-0000   | 0.0       | No attenuation (default) |
| 49           | 0011-0001   | - 0.5     |                          |
| 50           | 0011-0010   | - 1.0     |                          |
| 51           | 0011-0011   | - 1.5     |                          |
| :            | :           | :         |                          |
| 253          | 1111-1101   | - 102.5   |                          |
| 254          | 1111-1110   | - 103     | Negative maximum         |
| 255          | 1111-1111   | - ∞       | Negative infinite (Mute) |

Ramp-up frequency and ramp-down frequency can be controlled by Page 0, Register 63, D(7:6) and D(3:2) as shown in [Table 42](#). Also Ramp-up step and ramp-down step can be controlled by Page 0, Register 63 D(5:4) and D(1:0) as shown in [Table 43](#).

**Table 42. Ramp Up or Down Frequency**

| Ramp up speed | Every N f <sub>s</sub> | Comments | Ramp down frequency | Every N f <sub>s</sub> | Comments |
|---------------|------------------------|----------|---------------------|------------------------|----------|
| 00            | 1                      | Default  | 00                  | 1                      | Default  |
| 01            | 2                      |          | 01                  | 2                      |          |
| 10            | 4                      |          | 10                  | 4                      |          |

**Table 42. Ramp Up or Down Frequency (continued)**

|    |               |  |    |               |  |
|----|---------------|--|----|---------------|--|
| 11 | Direct change |  | 11 | Direct change |  |
|----|---------------|--|----|---------------|--|

**Table 43. Ramp Up or Down Step**

| Ramp up step | Step dB | Comments | Ramp down step | Step dB | Comments |
|--------------|---------|----------|----------------|---------|----------|
| 00           | 4.0     |          | 00             | -4.0    |          |
| 01           | 2.0     |          | 01             | -2.0    |          |
| 10           | 1.0     | Default  | 10             | -1.0    | Default  |
| 11           | 0.5     |          | 11             | -0.5    |          |

### Emergency Ramp Down

Digital volume emergency ramp down by is provided for situations such as I<sup>2</sup>S clock error and power supply failure. Ramp-down speed is controlled by Page 0, Register 64, D(7:6). Ramp-down step can be controlled by Page 0 Register 64, D(5:4). Default is ramp-down by every f<sub>s</sub> cycle with -4dB step.

### Zero Data Detect

The PCM512x has a zero-detect function. When the device detects the continuous zero data for both L-ch and R-cn, or separate L-cn and R-ch, Analog mutes are set to both OUTL and OUTR, or separate OUTL and OUTR. These are controlled by Page0, Register 65, D(2:1) as shown in [Table 44](#).

Continuous Zero data cycles are counted by LRCK, and the threshold of decision for analog mute can be set by Page 0, Register 59, D(6:4) for L-ch, and D(2:0) for Rch as shown in [Table 45](#). Default values are 0 for both channels.

In Hardware mode, the device uses default values.

**Table 44. Zero Detection Mode**

| ATMUTECTL | Value       | Function                                                    |
|-----------|-------------|-------------------------------------------------------------|
| Bit : 2   | 0           | Independently L-ch or R-ch are zero data for zero detection |
|           | 1 (Default) | Both L-ch and R-ch have to be zero data for zero detection  |
| Bit : 1   | 0           | Zero detection and analog mute are disabled for R-ch        |
|           | 1 (Default) | Zero detection analog mute are enabled for R-ch             |
| Bit : 0   | 0           | Zero detection analog mute are disabled for L-ch            |
|           | 1 (Default) | Zero detection analog mute are enabled for L-ch             |

**Table 45. Zero Data Detection Time**

| ATMUTETIML /<br>ATMUTETIMR | Number of LRCKs | Time @ 48kHz |
|----------------------------|-----------------|--------------|
| 0 0 0                      | 1024            | 21 ms        |
| 0 0 1                      | 5120            | 106 ms       |
| 0 1 0                      | 10240           | 213 ms       |
| 0 1 1                      | 25600           | 533 ms       |
| 1 0 0                      | 51200           | 1.066 sec    |
| 1 0 1                      | 102400          | 2.133 sec    |
| 1 1 0                      | 256000          | 5.333 sec    |
| 1 1 1                      | 512000          | 10.66 sec    |

## Power Save Modes

The PCM512x offers two power-save modes; standby and power-down.

When a clock error (SCK, BCK, and LRCK) or clock halt is detected, the PCM512x automatically enters standby mode. The DAC and line driver are also powered down. The device can also be placed in standby mode via software command.

When BCK and LRCK remain at a low level for more than 1 second, the PCM512x automatically enters power-down mode. Power-down mode disables the negative charge pump and bias/reference circuit, in addition to those disabled in standby mode. The device can also be placed in power-down mode via software command.

The detection time of BCK and LRCK halt can be controlled by Page 0, Register 44, D(2:0).

When expected Audio clocks (SCK, BCK, LRCK) are applied to the PCM512x, the device starts its powerup sequence automatically. The detection time for BCK and LRCK halt is programmable.

## Power Save Parameter Programming

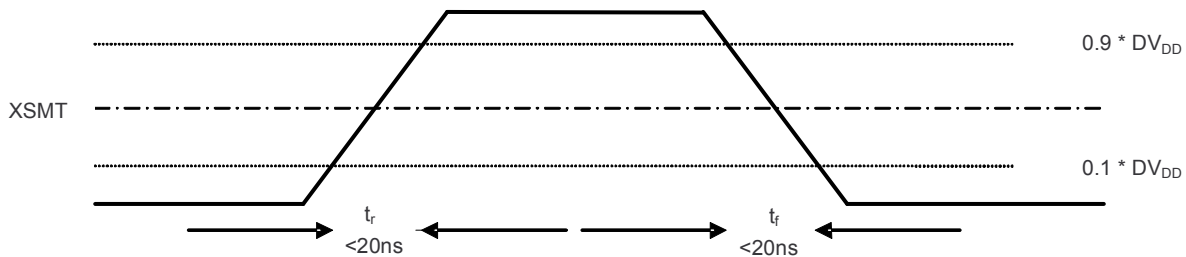
| Register                          | Description                                                                        |
|-----------------------------------|------------------------------------------------------------------------------------|
| Page 0, Register 2, D(4)          | Software standby mode command                                                      |
| Page 0, Register 2, D(0)          | Software power-down command                                                        |
| Page 0, Register 2, D(4) and D(0) | Software power-up sequence command (required after software standby or power-down) |
| Page 0, Register 44, D(2:0)       | Detection time of BCK and LRCK halt                                                |

### XSMT Pin (Soft Mute / Soft Un-Mute)

For external digital control of the PCM512x, the XSMT pin needs to be driven by an external digital host with a specific/minimum rising time ( $t_r$ ) and falling time ( $t_f$ ) for soft mute and soft un-mute. The PCM512x expects  $t_r/t_f$  times of less than 20ns. In the majority of applications, this shouldn't be a problem, however, traces with high capacitance may have issues.

When the XSMT pin is shifted from high to low (3.3V to 0V), a soft digital attenuation ramp is started. -1dB attenuation will be applied every sample time from 0dBFS to  $-\infty$ . The soft attenuation ramp takes 104 sample times.

When the XSMT pin is shifted from low to high (0V to 3.3V), a soft digital “un-mute” is started. 1dB gain steps are applied every sample time from  $-\infty$  to 0dBFS. The un-mute takes 104 sample times.



**Figure 77. XSMT Timing for Soft Mute and Soft Un-Mute**

**Table 46. XSMT Timing Parameters**

| Parameters          | Min | Max | Unit |
|---------------------|-----|-----|------|
| Rise time ( $t_r$ ) |     | 20  | ns   |
| Fall time ( $t_f$ ) |     | 20  | ns   |

### External Power Sense Undervoltage Protection mode (supported only when DVDD = 3.3V)

The XSMT pin can also be used to monitor a system voltage, such as the 24VDC LCD TV backlight, or 12VDC system supply using a voltage divider created with two resistors. (See [Figure 78](#) )

- If the XSMT pin makes a transition from “1” to “0” over 6ms or more, the device switches into external under-voltage protection mode. This mode uses two trigger levels.
- When the XSMT pin level reaches 2V, soft mute process begins.
- When the XSMT pin level reaches 1.2V, analog mute engages, regardless of digital audio level, and analog shutdown begins. (DAC and related circuitry powers down).

A timing diagram to show this is shown in [Figure 79](#).

#### NOTE

The XSMT input pin voltage range is from -0.3V to DVDD + 0.3V. The ratio of external resistors must produce a voltage within this input range. Any increase in power supply (such as power supply positive noise or ripple) can pull the XSMT pin higher than DVDD+0.3V.

For example, if the PCM512x is monitoring a 12V input, and dividing the voltage by 4, then the voltage at XSMT during ideal power supply conditions will be 3V. A voltage spike higher than 14.4V causes a voltage greater than 3.6V (DVDD+0.3) on the XSMT pin, potentially damaging the device.

Providing the divider is set appropriately, any DC voltage can be monitored.

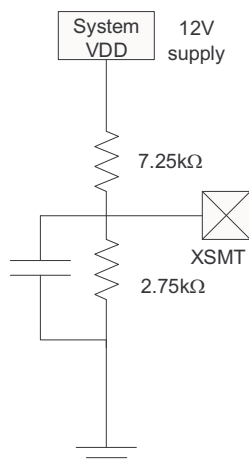


Figure 78. XSMT in External UVP Mode

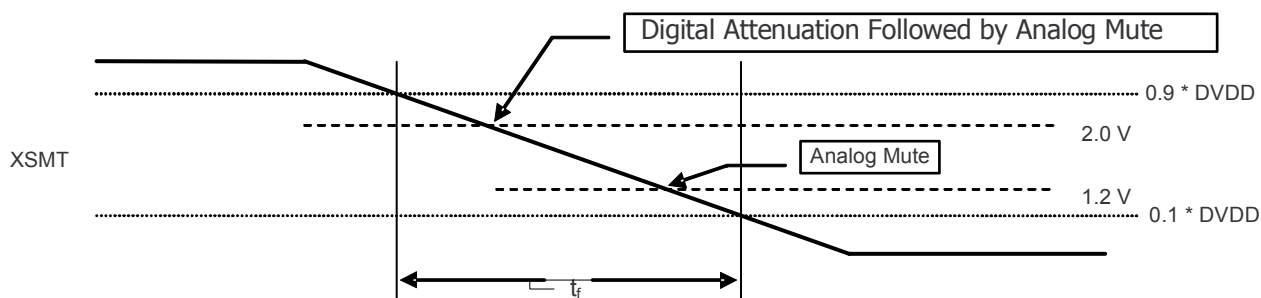


Figure 79. XSMT Timing for Undervoltage Protection

## Recommended Powerdown Sequence

With inadequate system design, the PCM512x can exhibit some pop on power down. Pops are caused by the device not having enough time to detect power loss and start the muting process.

The PCM512x evaluation board avoids audible pop with an electrolytic decoupling capacitor. This capacitor provides enough time between data loss from USB or S/PDIF and power supply loss for the muting process to take place.

The PCM512x has two auto-mute functions to mute the device upon power loss (intentional or unintentional).

### XSMT = 0

When the XSMT pin is pulled low, the incoming PCM data is attenuated to 0, closely followed by a hard analog mute. This process takes  $150t_s + 0.2\text{ms}$ .

As this mute time is mainly dominated by the sampling frequency, systems sampling at 192kHz will mute much faster than a 48kHz system.

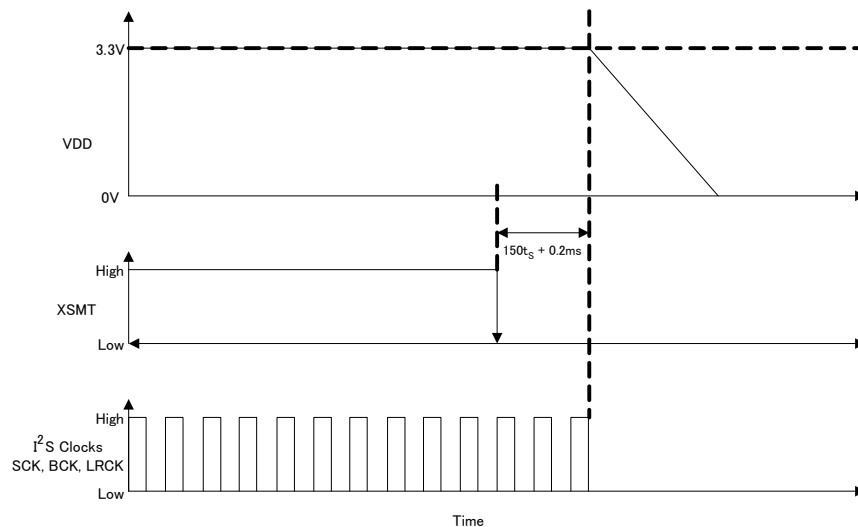
### Clock Error Detect

When clock error is detected on the incoming data clock, the PCM512x family switches to an internal oscillator, and continues to drive the DAC, while attenuating the data from the last known value. Once this process is complete, the PCM512x outputs will be hard muted to ground.

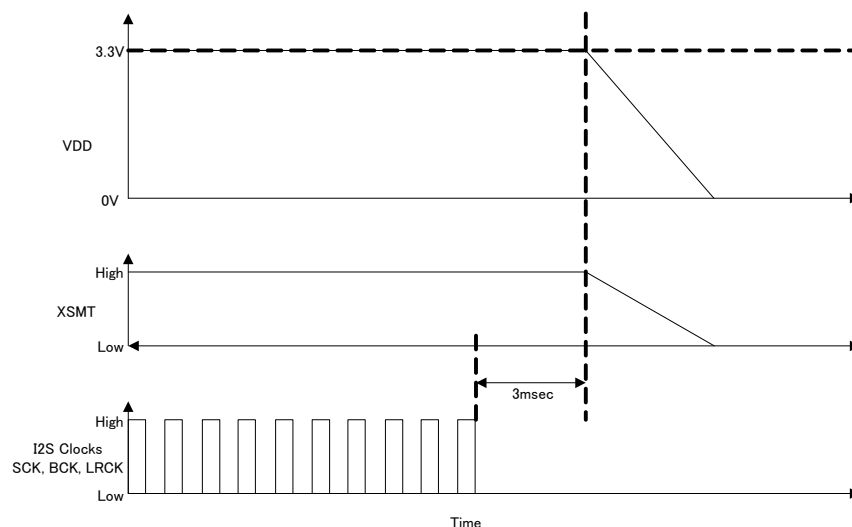
### Planned Shutdown

These auto-muting processes can be manipulated by system designs to mute before power loss in the following ways:

1. Assert XSMT low  $150t_s + 0.2\text{ms}$  before power is removed.

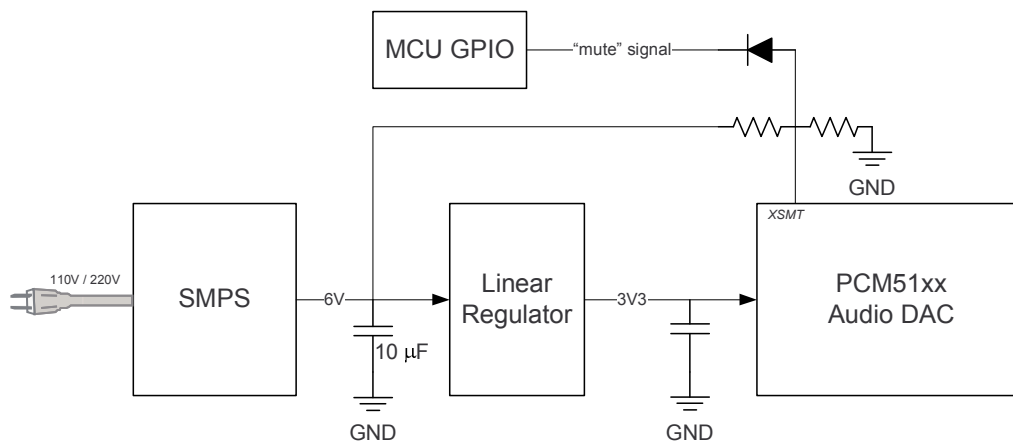


2. Stop I<sup>2</sup>S clocks (SCK, BCK, LRCK) 3ms before powerdown as shown below:



### Unplanned Shutdown

Many systems use a low-noise regulator to provide an AVDD 3.3V supply for the DAC. The XSMT Pin can take advantage of such a feature to measure the pre-regulated output from the system SMPS to mute the DAC before the entire SMPS discharges. [Figure 80](#) shows how to configure such a system to use the XSMT pin. The XSMT pin can also be used in parallel with a GPIO pin from the system microcontroller/DSP or Power Supply.



**Figure 80. Using the XSMT Pin**

### Software Control

#### SPI Interface

The SPI interface is a 4-wire synchronous serial port which operates asynchronously to the serial audio interface and the system clock (SCK). The serial control interface is used to program and read the on-chip mode registers.

The control interface includes MISO (pin 24), MOSI (pin 11), MC (pin 12), and MS (pin 18). MISO (Master In Slave Out) is the serial data output, used to read back the values of the mode registers; MOSI (Master Out Slave In) is the serial data input, used to program the mode registers.

MC is the serial bit clock, used to shift data in and out of the control port by falling edge of MC, and MS is the mode control enable with LOW active, used to enable the internal mode register access. If feedback from the device is not required, the MISO pin can be assigned to GPIO1 by register control.

## Register Read/Write Operation

All read/write operations for the serial control port use 16-bit data words. Figure 81 shows the control data word format. The most significant bit is the read/write bit. For write operations, the bit must be set to 0. For read operations, the bit must be set to 1. There are seven bits, labeled IDX[6:0], that hold the register index (or address) for the read and write operations. The least significant eight bits, D[7:0], contain the data to be written to, or the data that was read from, the register specified by IDX[6:0].

Figure 81 and Figure 82 show the functional timing diagram to write or read through the serial control port. MS is held at a logic-1 state until a register access. To start the register write or read cycle, set MS to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MOSI and read-back data on MISO. After the eighth clock cycle has completed, the data from the indexed-mode control register appears on MISO during the read operation. After the sixteenth clock cycle has completed, the data is latched into the indexed-mode control register during the write operation. To write or read subsequent data, MS is set to logic 1 once (See  $t_{MH}$  in Figure 86).

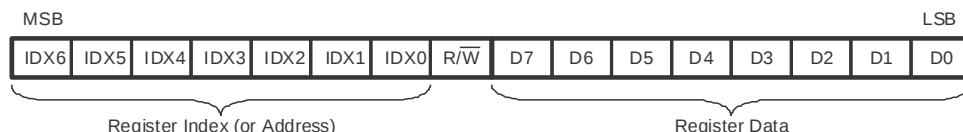


Figure 81. Control Data Word Format; MDI

### NOTE

B8 is used for selection of "Write" or "Read". Setting = 0 indicates a "Write", while = 1 indicates a "Read". Bits 15–9 are used for register address. Bits 7–0 are used for register data. Multiple-byte write or read (up to 8 bytes) is supported while MS is kept low. The address field becomes the initial address, automatically incrementing for each byte.

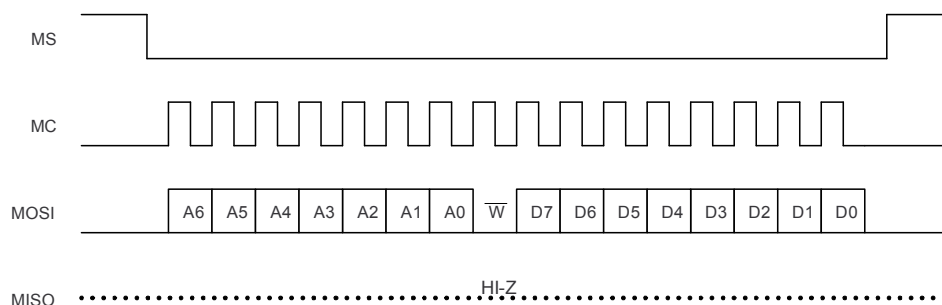


Figure 82. Serial Control Format; Write, Single Byte

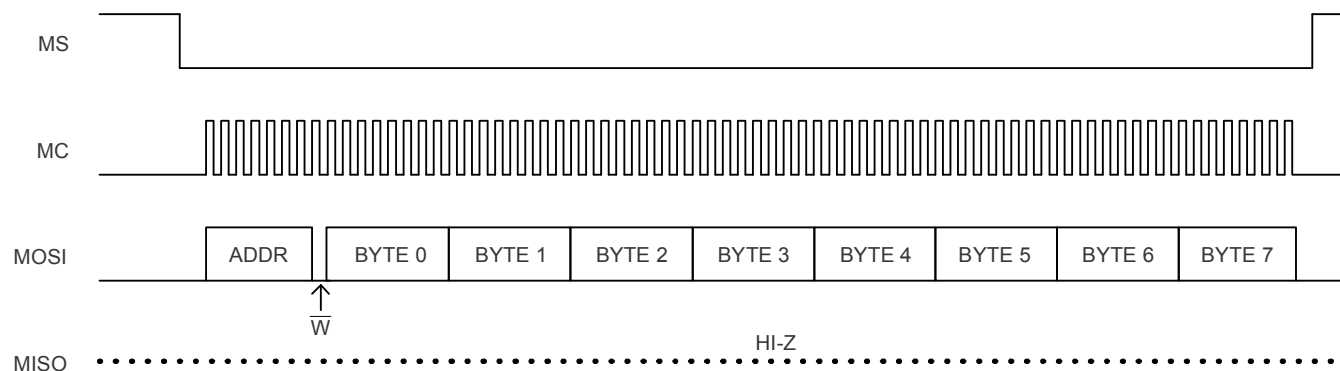
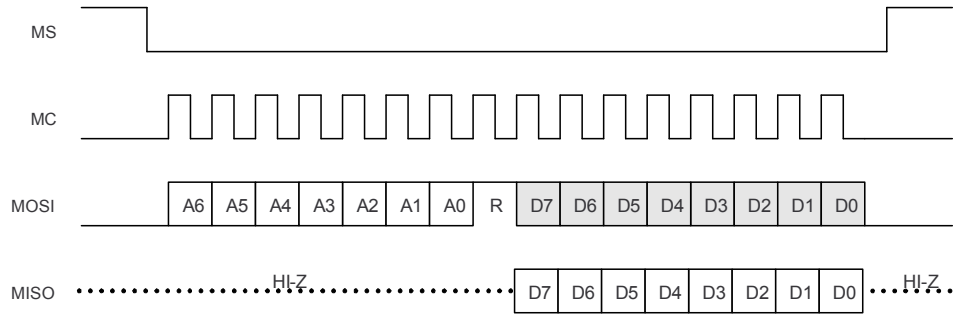
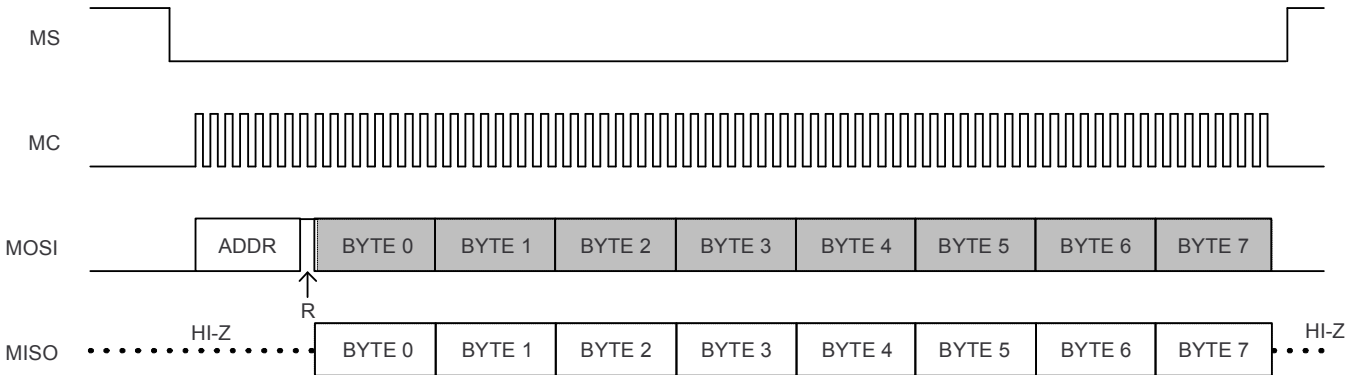


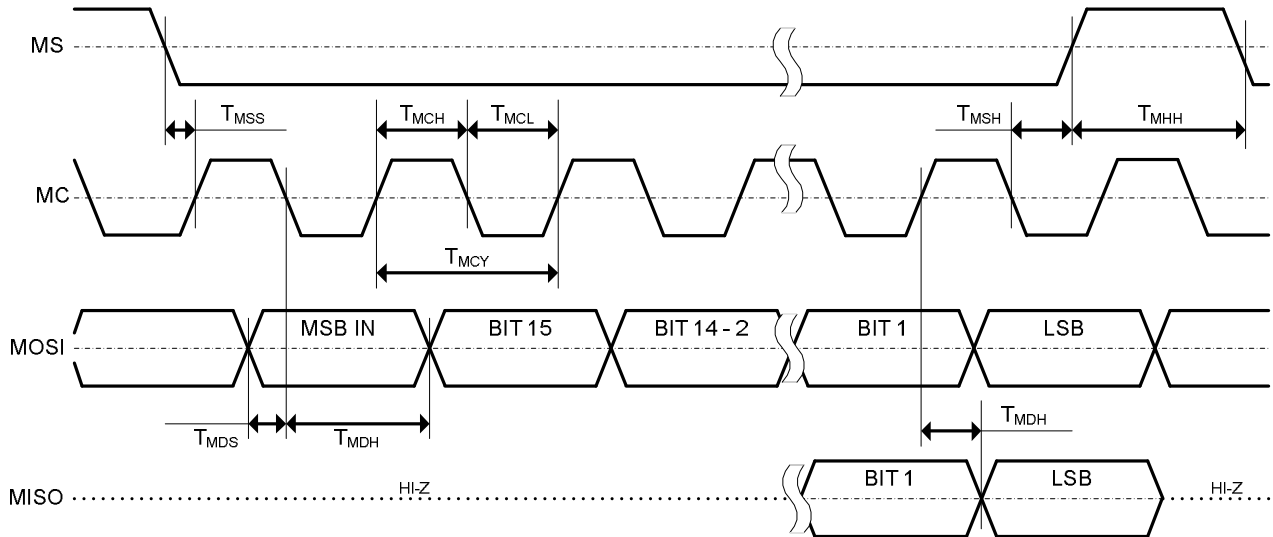
Figure 83. Serial Control Format; Write, Multiple Byte



**Figure 84. Serial Control Format; Read**



**Figure 85. Serial Control Format; Read, Multiple Byte**



**Figure 86. Control Interface Timing**

**Table 47. Control Interface Timing**

|           | Parameters                               | Min | Max | Units |
|-----------|------------------------------------------|-----|-----|-------|
| $t_{MCY}$ | MC Pulse Cycle Time                      | 100 |     | ns    |
| $t_{MCL}$ | MC Low Level Time                        | 40  |     |       |
| $t_{MCH}$ | MC High Level Time                       | 40  |     |       |
| $t_{MHH}$ | $\overline{MS}$ High Level Time          | 20  |     |       |
| $t_{MSS}$ | $\overline{MS}$ ↓ Edge to MC ↑ Edge      | 30  |     |       |
| $t_{MSH}$ | $\overline{MS}$ Hold Time <sup>(1)</sup> | 30  |     |       |
| $t_{MDH}$ | MDI Hold Time                            | 15  |     |       |
| $t_{MDS}$ | MDI Set-up Time                          | 15  |     |       |
| $t_{MOS}$ | MC Rise Edge to MDO Stable               |     | 20  |       |

(1) MC falling edge for LSB to MS rising edge.

## I<sup>2</sup>C Interface

The PCM512x supports the I<sup>2</sup>C serial bus and the data transmission protocol for standard and fast mode as a slave device. This protocol is explained in the I<sup>2</sup>C specification 2.0.

In I<sup>2</sup>C mode, the control terminals are changed as follows.

**Table 48. I<sup>2</sup>C Pins and Functions**

| Signal | Pin | I/O | Description                |
|--------|-----|-----|----------------------------|
| SDA    | 11  | I/O | I <sup>2</sup> C data      |
| SCL    | 12  | I   | I <sup>2</sup> C clock     |
| ADR2   | 16  | I   | I <sup>2</sup> C address 2 |
| ADR1   | 24  | I   | I <sup>2</sup> C address 1 |

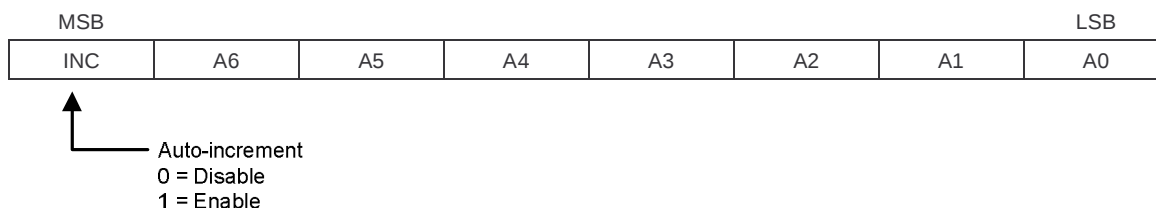
## Slave Address

**Table 49. I<sup>2</sup>C Slave Address**

| MSB |   |   |   |   |      |      | LSB               |
|-----|---|---|---|---|------|------|-------------------|
| 1   | 0 | 0 | 1 | 1 | ADR2 | ADR1 | R/ $\overline{W}$ |

The PCM512x has 7 bits for its own slave address. The first five bits (MSBs) of the slave address are factory preset to 10011. The next two bits of the address byte are the device select bits which can be user-defined by the ADR1 and ADR0 terminals. A maximum of four PCM51xxs can be connected on the same bus at one time. Each PCM512x responds when it receives its own slave address.

## Register Address Auto-Increment Mode

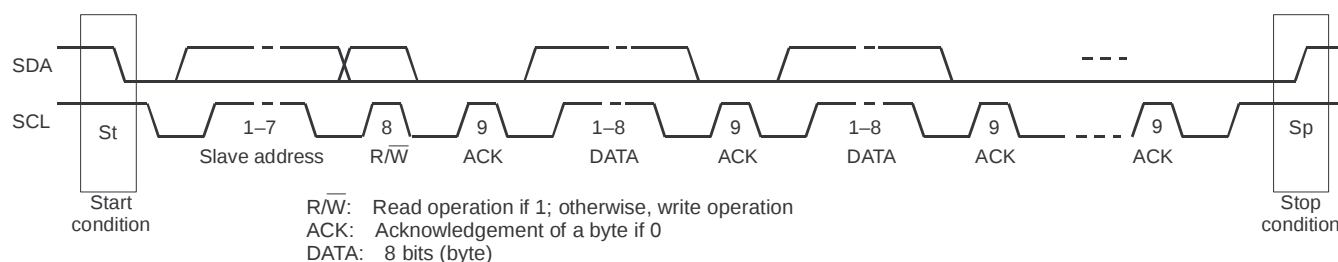


**Figure 87. Auto Increment Mode**

Auto-increment mode allows multiple sequential register locations to be written to or read back in a single operation, and is especially useful for block write and read operations.

## Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The PCM512x supports only slave receivers and slave transmitters.



**Figure 88. Packet Protocol**

**Table 50. Write Operation - Basic I<sup>2</sup>C Framework**

|             |    |               |    |     |      |     |      |     |  |     |    |
|-------------|----|---------------|----|-----|------|-----|------|-----|--|-----|----|
| Transmitter | M  | M             | M  | S   | M    | S   | M    | S   |  | S   | M  |
| Data Type   | St | slave address | R/ | ACK | DATA | ACK | DATA | ACK |  | ACK | Sp |

**Table 51. Read Operation - Basic I<sup>2</sup>C Framework**

|             |    |               |    |     |      |     |      |     |  |      |    |
|-------------|----|---------------|----|-----|------|-----|------|-----|--|------|----|
| Transmitter | M  | M             | M  | S   | S    | M   | S    | M   |  | M    | M  |
| Data Type   | St | slave address | R/ | ACK | DATA | ACK | DATA | ACK |  | NACK | Sp |

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition

### Write Register

A master can write to any PCM512x registers using single or multiple accesses. The master sends a PCM512x slave address with a write bit, a register address with auto-increment bit, and the data. If auto-increment is enabled, the address is that of the starting register, followed by the data to be transferred. When the data is received properly, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. [Table 52](#) shows the write operation.

**Table 52. Write Operation**

|             |    |            |   |     |     |          |     |              |     |              |     |  |     |    |
|-------------|----|------------|---|-----|-----|----------|-----|--------------|-----|--------------|-----|--|-----|----|
| Transmitter | M  | M          | M | S   | M   |          | S   | M            | S   | M            | S   |  | S   | M  |
| Data Type   | St | slave addr | W | ACK | inc | reg addr | ACK | write data 1 | ACK | write data 2 | ACK |  | ACK | Sp |

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition; W = Write; ACK = Acknowledge

### Read Register

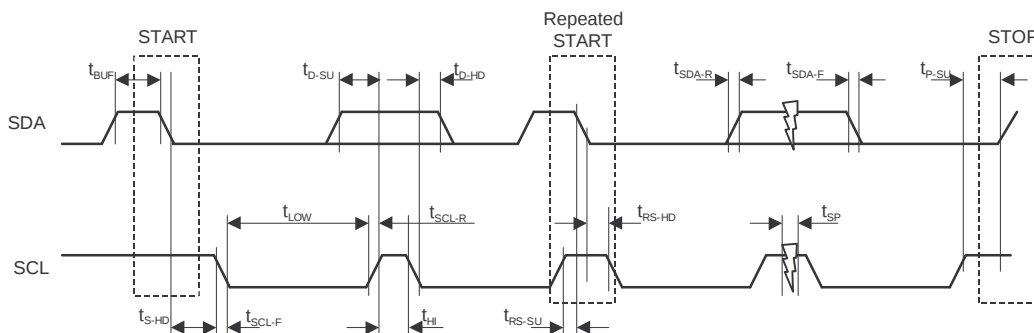
A master can read the PCM512x register. The value of the register address is stored in an indirect index register in advance. The master sends a PCM512x slave address with a read bit after storing the register address. Then the PCM512x transfers the data which the index register points to. When auto-increment is enabled, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. [Table 53](#) shows the read operation.

**Table 53. Read Operation**

|             |    |            |   |     |     |          |     |    |            |   |     |      |     |  |      |    |
|-------------|----|------------|---|-----|-----|----------|-----|----|------------|---|-----|------|-----|--|------|----|
| Transmitter | M  | M          | M | S   | M   |          | S   | M  | M          | M | S   | S    | M   |  | M    | M  |
| Data Type   | St | slave addr | W | ACK | inc | reg addr | ACK | Sr | slave addr | R | ACK | data | ACK |  | NACK | Sp |

M = Master Device; S = Slave Device; St = Start Condition; Sr = Repeated start condition; Sp = Stop Condition; W = Write; R = Read; NACK = Not acknowledge

### Timing Characteristics


**Figure 89. Register Access Timing**

**Table 54. I<sup>2</sup>C Bus Timing**

| SYMBOL              | PARAMETER                                                                             | CONDITIONS | MIN                    | MAX  | UNIT |
|---------------------|---------------------------------------------------------------------------------------|------------|------------------------|------|------|
| f <sub>SCL</sub>    | SCL clock frequency                                                                   | Standard   |                        | 100  | kHz  |
|                     |                                                                                       | Fast       |                        | 400  | kHz  |
| t <sub>BUF</sub>    | Bus free time between a STOP and START condition                                      | Standard   | 4.7                    |      | μs   |
|                     |                                                                                       | Fast       | 1.3                    |      |      |
| t <sub>LOW</sub>    | Low period of the SCL clock                                                           | Standard   | 4.7                    |      | μs   |
|                     |                                                                                       | Fast       | 1.3                    |      |      |
| t <sub>HI</sub>     | High period of the SCL clock                                                          | Standard   | 4.0                    |      | μs   |
|                     |                                                                                       | Fast       | 600                    |      | ns   |
| t <sub>RS-SU</sub>  | Setup time for (repeated)START condition                                              | Standard   | 4.7                    |      | μs   |
|                     |                                                                                       | Fast       | 600                    |      | ns   |
| t <sub>S-HD</sub>   | Hold time for (repeated)START condition                                               | Standard   | 4.0                    |      | μs   |
| t <sub>RS-HD</sub>  |                                                                                       | Fast       | 600                    |      | ns   |
| t <sub>D-SU</sub>   | Data setup time                                                                       | Standard   | 250                    |      | ns   |
|                     |                                                                                       | Fast       | 100                    |      |      |
| t <sub>D-HD</sub>   | Data hold time                                                                        | Standard   | 0                      | 900  | ns   |
|                     |                                                                                       | Fast       | 0                      | 900  |      |
| t <sub>SCL-R</sub>  | Rise time of SCL signal                                                               | Standard   | 20 + 0.1C <sub>B</sub> | 1000 | ns   |
|                     |                                                                                       | Fast       | 20 + 0.1C <sub>B</sub> | 300  |      |
| t <sub>SCL-R1</sub> | Rise time of SCL signal after a repeated START condition and after an acknowledge bit | Standard   | 20 + 0.1C <sub>B</sub> | 1000 | ns   |
|                     |                                                                                       | Fast       | 20 + 0.1C <sub>B</sub> | 300  |      |
| t <sub>SCL-F</sub>  | Fall time of SCL signal                                                               | Standard   | 20 + 0.1C <sub>B</sub> | 1000 | ns   |
|                     |                                                                                       | Fast       | 20 + 0.1C <sub>B</sub> | 300  |      |
| t <sub>SDA-R</sub>  | Rise time of SDA signal                                                               | Standard   | 20 + 0.1C <sub>B</sub> | 1000 | ns   |
|                     |                                                                                       | Fast       | 20 + 0.1C <sub>B</sub> | 300  |      |
| t <sub>SDA-F</sub>  | Fall time of SDA signal                                                               | Standard   | 20 + 0.1C <sub>B</sub> | 1000 | ns   |
|                     |                                                                                       | Fast       | 20 + 0.1C <sub>B</sub> | 300  |      |
| t <sub>P-SU</sub>   | Setup time for STOP condition                                                         | Standard   | 4.0                    |      | μs   |
|                     |                                                                                       | Fast       | 600                    |      | ns   |
| C <sub>B</sub>      | Capacitive load for SDA and SCL line                                                  |            |                        | 400  | pF   |
| t <sub>SP</sub>     | Pulse width of spike suppressed                                                       | Fast       |                        | 50   | ns   |
| V <sub>NH</sub>     | Noise margin at High level for each connected device (including hysteresis)           |            | 0.2V <sub>DD</sub>     |      | V    |

## PCM512x Register Map

In any page, register 0 is the Page Select Register. The register value selects the Register Page from 0 to 255 for next read or write command.

**Table 55. Register Map Summary**

| Register Number | Description                                                    |
|-----------------|----------------------------------------------------------------|
| <b>Page 0</b>   |                                                                |
| 0               | Control register                                               |
| 1               | Analog control register                                        |
| 2               | Standby, Powerdown requests                                    |
| 3               | Mute                                                           |
| 4               | PLL Lock Flag, PLL enable                                      |
| 5               | Reserved                                                       |
| 6               | SPI MISO function select                                       |
| 7               | De-emphasis enable, SDOUT select                               |
| 8               | GPIO enables                                                   |
| 9               | BCK, LRCLK configuration                                       |
| 10              | DSP GPIO Input                                                 |
| 11              | Reserved                                                       |
| 12              | Master mode BCK, LRCLK reset                                   |
| 13              | PLL clock source select                                        |
| 14 - 19         | Reserved                                                       |
| 20 - 24         | PLL dividers                                                   |
| 25, 26          | Reserved                                                       |
| 27              | DSP clock divider                                              |
| 28              | DAC clock divider                                              |
| 29              | NCP clock divider                                              |
| 30              | OSR clock divider                                              |
| 31              | Reserved                                                       |
| 32, 33          | Master mode dividers                                           |
| 34              | $f_s$ speed mode                                               |
| 35, 36          | IDAC (number of DSP clock cycles available in one audio frame) |
| 37              | Ignore various errors                                          |
| 38,39           | Reserved                                                       |

**Table 55. Register Map Summary (continued)**

|                |                                                                              |
|----------------|------------------------------------------------------------------------------|
| 40, 41         | I <sup>2</sup> S configuration                                               |
| 42             | DAC data path                                                                |
| 43             | DSP program selection                                                        |
| 44             | Clock missing detection period                                               |
| 59             | Auto mute time                                                               |
| 60 - 64        | Digital volume                                                               |
| 65             | Auto mute                                                                    |
| 75 - 79        | Reserved                                                                     |
| 80 - 85        | GPIO output selection                                                        |
| 86, 87         | GPIO control                                                                 |
| 88, 89         | Reserved                                                                     |
| 90             | DSP overflow                                                                 |
| 91 - 94        | Sample rate status                                                           |
| 95 - 107       | Reserved                                                                     |
| 108            | Analog mute monitor                                                          |
| 109 - 118      | Reserved                                                                     |
| 119            | GPIO input                                                                   |
| 120            | Auto Mute flags                                                              |
| <b>Page 1</b>  |                                                                              |
| 1              | Output amplitude type                                                        |
| 2              | Analog gain control                                                          |
| 3, 4           | Reserved                                                                     |
| 5              | Undervoltage protection                                                      |
| 6              | Analog mute control                                                          |
| 7              | Analog gain boost                                                            |
| 8, 9           | VCOM configuration                                                           |
| <b>Page 44</b> |                                                                              |
| 1              | Coefficient memory (CRAM) control                                            |
| Pages 44 - 52  | Coefficient buffer - A (256 coeffs x 24 bits) : See <a href="#">Table 56</a> |
| Pages 66 - 74  | Coefficient buffer - B (256 coeffs x 24 bits) : See <a href="#">Table 57</a> |

**Table 56. Coefficient Buffer-A Map**

| Coeff NO | Page NO | Base Register | Base Register+0 | Base Register+1 | Base Register+2 | Base Register+3 |
|----------|---------|---------------|-----------------|-----------------|-----------------|-----------------|
| C0       | 44      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C1       | 44      | 12            | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C29      | 44      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C30      | 45      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C59      | 45      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C60      | 46      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C89      | 46      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C90      | 47      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |

**Table 56. Coefficient Buffer-A Map (continued)**

|      |    |     |             |            |           |           |
|------|----|-----|-------------|------------|-----------|-----------|
| ..   | .. | ..  | ..          | ..         | ..        | ..        |
| C119 | 47 | 124 | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |
| C120 | 48 | 8   | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |
| ..   | .. | ..  | ..          | ..         | ..        | ..        |
| C149 | 48 | 124 | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |
| C150 | 49 | 8   | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |
| ..   | .. | ..  | ..          | ..         | ..        | ..        |
| C179 | 49 | 124 | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |
| C180 | 50 | 8   | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |
| ..   | .. | ..  | ..          | ..         | ..        | ..        |
| C209 | 50 | 124 | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |
| C210 | 51 | 8   | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |
| ..   | .. | ..  | ..          | ..         | ..        | ..        |
| C239 | 51 | 124 | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |
| C240 | 52 | 8   | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |
| ..   | .. | ..  | ..          | ..         | ..        | ..        |
| C255 | 52 | 68  | Coef(23:16) | Coef(15:8) | Coef(7:0) | Reserved. |

**Table 57. Coefficient Buffer-B Map**

| Coeff NO | Page NO | Base Register | Base Register+0 | Base Register+1 | Base Register+2 | Base Register+3 |
|----------|---------|---------------|-----------------|-----------------|-----------------|-----------------|
| C0       | 62      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C1       | 62      | 12            | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C29      | 62      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C30      | 63      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C59      | 63      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C60      | 64      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C89      | 64      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C90      | 65      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C119     | 65      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C120     | 66      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C149     | 66      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C150     | 67      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C179     | 67      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C180     | 68      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C209     | 68      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C210     | 69      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C239     | 69      | 124           | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| C240     | 70      | 8             | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |
| ..       | ..      | ..            | ..              | ..              | ..              | ..              |
| C255     | 70      | 68            | Coef(23:16)     | Coef(15:8)      | Coef(7:0)       | Reserved.       |

## Detailed Register Descriptions

### Page 0 / Register 1

| Dec         | Hex | b7  | b6  | b5  | b4   | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|------|-----|-----|-----|------|
| 1           | 01  | RSV | RSV | RSV | RSTM | RSV | RSV | RSV | RSTR |
| Reset Value |     |     |     |     | 0    |     |     |     | 0    |

|             |                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                       |
| <b>RSTM</b> | <b>Reset Modules</b><br>This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coefficient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in standby mode.<br>Default value: 0<br>0: Normal<br>1: Reset modules                                                                                                |
| <b>RSTR</b> | <b>Reset Registers</b><br>This bit resets the mode registers back to their initial values. The RAM content is not cleared, but the execution source will be back to ROM. This bit is auto cleared and must be set only when the DAC is in standby mode (resetting registers when the DAC is running is prohibited and not supported).<br>Default value: 0<br>0: Normal<br>1: Reset mode registers |

### Page 0 / Register 2

| Dec         | Hex | b7  | b6  | b5  | b4   | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|------|-----|-----|-----|------|
| 2           | 02  | RSV | RSV | RSV | RQST | RSV | RSV | RSV | RQPD |
| Reset Value |     |     |     |     | 0    |     |     |     | 0    |

|             |                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                              |
| <b>RQST</b> | <b>Standby Request</b><br>When this bit is set, the DAC is forced into system standby mode, which is also the mode the system enters in case of clock errors. In this mode, most subsystems are powered down except for the charge pump and digital power supply.<br>Default value: 0<br>0: Normal operation<br>1: Standby mode                                                                                          |
| <b>RQPD</b> | <b>Powerdown Request</b><br>Setting RQPD sends the DAC into powerdown mode, reducing power consumption to a minimum. The charge pump also powers down. However, it takes longer to restart from this mode. Powerdown mode has higher precedence than standby mode; setting this bit along with bit 4 for standby mode sends the DAC into powerdown mode.<br>Default value: 0<br>0: Normal operation<br>1: Powerdown mode |

### Page 0 / Register 3

| Dec         | Hex | b7  | b6  | b5  | b4   | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|------|-----|-----|-----|------|
| 3           | 03  | RSV | RSV | RSV | RQML | RSV | RSV | RSV | RQMR |
| Reset Value |     |     |     |     | 0    |     |     |     | 0    |

|             |                                                                                                                                                                                                                         |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                             |
| <b>RQML</b> | <b>Mute Left Channel</b><br>This bit issues soft mute request for the left channel. The volume will be smoothly ramped down or up to avoid pop or click noise.<br><br>Default value: 0<br>0: Normal volume<br>1: Mute   |
| <b>RQMR</b> | <b>Mute Right Channel</b><br>This bit issues soft mute request for the right channel. The volume will be smoothly ramped down or up to avoid pop or click noise.<br><br>Default value: 0<br>0: Normal volume<br>1: Mute |

**Page 0 / Register 4**

| Dec         | Hex | b7  | b6  | b5  | b4   | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|------|-----|-----|-----|------|
| 4           | 04  | RSV | RSV | RSV | PLCK | RSV | RSV | RSV | PLLE |
| Reset Value |     |     |     |     |      |     |     |     | 1    |

|             |                                                                                                                                                                                                                          |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                              |
| <b>PLCK</b> | <b>PLL Lock Flag (Read Only)</b><br>This bit indicates whether the PLL is locked or not. When the PLL is disabled this bit always shows that the PLL is not locked. 0: The PLL is locked<br><br>1: The PLL is not locked |
| <b>PLLE</b> | <b>PLL Enable</b><br>This bit enables or disables the internal PLL. When PLL is disabled, the master clock will be switched to the SCK.<br><br>Default value: 1<br>0: Disable PLL<br>1: Enable PLL                       |

**Page 0 / Register 6**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-----|-----|-------|-------|
| 6           | 06  | RSV | RSV | RSV | RSV | RSV | RSV | FSMI1 | FSMI0 |
| Reset Value |     |     |     |     |     |     |     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                  |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                      |
| <b>FSMI[1:0]</b> | <b>SPI MISO function sel</b><br>These bits select the function of the SPI_MISO pin when in SPI mode. If the pin is set as GPIO, register readout via SPI is not possible.<br><br>Default value: 00<br>00: SPI_MISO<br>01: GPIO1<br>Others: Reserved (Do not set) |

**Page 0 / Register 7**

| Dec         | Hex | b7  | b6  | b5  | b4   | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|------|-----|-----|-----|------|
| 7           | 07  | RSV | RSV | RSV | DEMP | RSV | RSV | RSV | SDSL |
| Reset Value |     |     |     |     | 0    |     |     |     | 0    |

|             |                                                                                                                                                                                                                                                                                                                 |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                     |
| <b>DEMP</b> | <b>De-Emphasis Enable</b><br>This bit enables or disables the de-emphasis filter. The default coefficients are for 44.1kHz sampling rate, but can be changed by reprogramming the appropriate coefficients in RAM.<br>Default value: 0<br>0: De-emphasis filter is disabled<br>1: De-emphasis filter is enabled |
| <b>SDSL</b> | <b>SDOUT Select</b><br>This bit selects what is being output as SDOUT via GPIO pins.<br>Default value: 0<br>0: SDOUT is the DSP output (post-processing)<br>1: SDOUT is the DSP input (pre-processing)                                                                                                          |

**Page 0 / Register 8**

| Dec         | Hex | b7  | b6  | b5   | b4   | b3   | b2   | b1   | b0   |
|-------------|-----|-----|-----|------|------|------|------|------|------|
| 8           | 08  | RSV | RSV | G6OE | G5OE | G4OE | G3OE | G2OE | G1OE |
| Reset Value |     |     |     | 0    | 0    | 0    | 0    | 0    | 0    |

|             |                                                                                                                                           |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                               |
| <b>G6OE</b> | <b>GPIO6 Output Enable</b><br>This bit sets the direction of the GPIO6 pin<br>Default value: 0<br>0: GPIO6 is input<br>1: GPIO6 is output |
| <b>G5OE</b> | <b>GPIO5 Output Enable</b><br>This bit sets the direction of the GPIO5 pin<br>Default value: 0<br>0: GPIO5 is input<br>1: GPIO5 is output |
| <b>G4OE</b> | <b>GPIO4 Output Enable</b><br>This bit sets the direction of the GPIO4 pin<br>Default value: 0<br>0: GPIO4 is input<br>1: GPIO4 is output |
| <b>G3OE</b> | <b>GPIO3 Output Enable</b><br>This bit sets the direction of the GPIO3 pin<br>Default value: 0<br>0: GPIO3 is input<br>1: GPIO3 is output |
| <b>G2OE</b> | <b>GPIO2 Output Enable</b><br>This bit sets the direction of the GPIO2 pin<br>Default value: 0                                            |

|             |                                                                                                                                           |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------|
|             | 0: GPIO2 is input<br>1: GPIO2 is output                                                                                                   |
| <b>G1OE</b> | <b>GPIO1 Output Enable</b><br>This bit sets the direction of the GPIO1 pin<br>Default value: 0<br>0: GPIO1 is input<br>1: GPIO1 is output |

**Page 0 / Register 9**

| Dec         | Hex | b7  | b6  | b5   | b4   | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|------|------|-----|-----|-----|------|
| 9           | 09  | RSV | RSV | BCKP | BCKO | RSV | RSV | RSV | LRKO |
| Reset Value |     |     |     | 0    | 0    |     |     |     | 0    |

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>BCKP</b> | <b>BCK Polarity</b><br>This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally they are assumed to be aligned to the falling edge of the BCK.<br>Default value: 0<br>0: Normal BCK mode<br>1: Inverted BCK mode                                                                                                                                                                                                                     |
| <b>BCKO</b> | <b>BCK Output Enable</b><br>This bit sets the BCK pin direction to output for I <sup>2</sup> S master mode operation. In I <sup>2</sup> S master mode the PCM51xx outputs the reference BCK and LRCK, and the external source device provides the DIN according to these clocks. Use Page 0 / Register 32 to program the division factor of the SCK to yield the desired BCK rate (normally 64f <sub>s</sub> )<br>Default value: 0<br>0: BCK is input (I <sup>2</sup> S slave mode)<br>1: BCK is output (I <sup>2</sup> S master mode) |
| <b>LRKO</b> | <b>LRCLK Output Enable</b><br>This bit sets the LRCK pin direction to output for I <sup>2</sup> S master mode operation. In I <sup>2</sup> S master mode the PCM51xx outputs the reference BCK and LRCK, and the external source device provides the DIN according to these clocks. Use Page 0 / Register 33 to program the division factor of the BCK to yield 1f <sub>s</sub> for LRCK.<br>Default value: 0<br>0: LRCK is input (I <sup>2</sup> S slave mode)<br>1: LRCK is output (I <sup>2</sup> S master mode)                    |

**Page 0 / Register 10**

| Dec         | Hex | b7    | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| 10          | 0A  | DSPG7 | DSPG6 | DSPG5 | DSPG4 | DSPG3 | DSPG2 | DSPG1 | DSPG0 |
| Reset Value |     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                         |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DSPG[7:0]</b> | <b>DSP GPIO Input</b><br>The DSP accepts a 24-bit external control signals input. The value set in this register will go to bit 16:8 of this external input.<br>Default value: 00000000 |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**Page 0 / Register 12**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1   | b0   |
|-------------|-----|-----|-----|-----|-----|-----|-----|------|------|
| 12          | 0C  | RSV | RSV | RSV | RSV | RSV | RSV | RBCK | RLRK |
| Reset Value |     |     |     |     |     |     |     | 0    | 0    |

|             |                                                                                                                                                                                                                                                                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                          |
| <b>RBCK</b> | <b>Master Mode BCK Divider Reset</b><br>This bit, when set to 0, will reset the SCK divider to generate BCK clock for I <sup>2</sup> S master mode. To use I <sup>2</sup> S master mode, the divider must be enabled and programmed properly.<br>Default value: 0<br>0: Master mode BCK clock divider is reset<br>1: Master mode BCK clock divider is functional     |
| <b>RLRK</b> | <b>Master Mode LRCK Divider Reset</b><br>This bit, when set to 0, will reset the BCK divider to generate LRCK clock for I <sup>2</sup> S master mode. To use I <sup>2</sup> S master mode, the divider must be enabled and programmed properly.<br>Default value: 0<br>0: Master mode LRCK clock divider is reset<br>1: Master mode LRCK clock divider is functional |

**Page 0 / Register 13**

| Dec         | Hex | b7  | b6  | b5  | b4   | b3  | b2  | b1  | b0  |
|-------------|-----|-----|-----|-----|------|-----|-----|-----|-----|
| 13          | 0D  | RSV | RSV | RSV | SREF | RSV | RSV | RSV | RSV |
| Reset Value |     |     |     |     | 0    |     |     |     |     |

|             |                                                                                                                                                                                                                                     |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                         |
| <b>SREF</b> | <b>PLL Reference</b><br>This bit select the source clock for internal PLL. This bit is ignored and overridden in clock auto set mode.<br>Default value: 0<br>0: The PLL reference clock is SCK<br>1: The PLL reference clock is BCK |

**Page 0 / Register 20**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-------|-------|-------|-------|
| 20          | 14  | RSV | RSV | RSV | RSV | PPDV3 | PPDV2 | PPDV1 | PPDV0 |
| Reset Value |     |     |     |     |     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                           |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                               |
| <b>PPDV[3:0]</b> | <b>PLL P</b><br>These bits set the PLL divider P factor. These bits are ignored in clock auto set mode.<br>Default value: 0000<br>0000: P=1<br>0001: P=2<br>...<br>1110: P=15<br>1111: Prohibited (do not set this value) |

**Page 0 / Register 21**

| Dec         | Hex | b7  | b6  | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-------|-------|-------|-------|-------|-------|
| 21          | 15  | RSV | RSV | PJDV5 | PJDV4 | PJDV3 | PJDV2 | PJDV1 | PJDV0 |
| Reset Value |     |     |     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                            |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                |
| <b>PJDV[5:0]</b> | <b>PLL J</b><br>These bits set the J part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.<br><br>Default value: 000000<br>000000: Prohibited (do not set this value)<br>000001: J=1<br>000010: J=2<br>...<br>111111: J=63 |

**Page 0 / Register 22**

| Dec         | Hex | b7  | b6  | b5     | b4     | b3     | b2     | b1    | b0    |
|-------------|-----|-----|-----|--------|--------|--------|--------|-------|-------|
| 22          | 16  | RSV | RSV | PDDV13 | PDDV12 | PDDV11 | PDDV10 | PDDV9 | PDDV8 |
| Reset Value |     |     |     | 0      | 0      | 0      | 0      | 0     | 0     |

**Page 0 / Register 23**

| 23          | 17 | PDDV7 | PDDV6 | PDDV5 | PDDV4 | PDDV3 | PDDV2 | PDDV1 | PDDV0 |
|-------------|----|-------|-------|-------|-------|-------|-------|-------|-------|
| Reset Value |    | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

|                   |                                                                                                                                                                                                                                                                                                                    |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>        | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                        |
| <b>PDDV[13:0]</b> | <b>PLL D (MSB)</b><br>These bits set the D part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.<br><br>Default value: 0000000000000000<br>0 (in decimal): D=0000<br>1 (in decimal): D=0001<br>...<br>9999 (in decimal): D=9999<br>others: Prohibited (do not set) |

**Page 0 / Register 24**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-------|-------|-------|-------|
| 24          | 18  | RSV | RSV | RSV | RSV | PRDV3 | PRDV2 | PRDV1 | PRDV0 |
| Reset Value |     |     |     |     |     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                      |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                          |
| <b>PRDV[3:0]</b> | <b>PLL R</b><br>These bits set the R part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.<br><br>Default value: 0000<br>0000: R=1<br>0001: R=2<br>...<br>1111: R=16 |

**Page 0 / Register 27**

| Dec         | Hex | b7  | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-------|-------|-------|-------|-------|-------|-------|
| 27          | 1B  | RSV | DDSP6 | DDSP5 | DDSP4 | DDSP3 | DDSP2 | DDSP1 | DDSP0 |
| Reset Value |     |     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                        |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                            |
| <b>DDSP[6:0]</b> | <b>DSP Clock Divider</b><br>These bits set the source clock divider value for the DSP clock. These bits are ignored in clock auto set mode.<br>Default value: 0000000<br>0000000: Divide by 1<br>0000001: Divide by 2<br>...<br>1111111: Divide by 128 |

**Page 0 / Register 28**

| Dec         | Hex | b7  | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-------|-------|-------|-------|-------|-------|-------|
| 28          | 1C  | RSV | DDAC6 | DDAC5 | DDAC4 | DDAC3 | DDAC2 | DDAC1 | DDAC0 |
| Reset Value |     |     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                        |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                            |
| <b>DDAC[6:0]</b> | <b>DAC Clock Divider</b><br>These bits set the source clock divider value for the DAC clock. These bits are ignored in clock auto set mode.<br>Default value: 0000000<br>0000000: Divide by 1<br>0000001: Divide by 2<br>...<br>1111111: Divide by 128 |

**Page 0 / Register 29**

| Dec         | Hex | b7  | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-------|-------|-------|-------|-------|-------|-------|
| 29          | 1D  | RSV | DNCP6 | DNCP5 | DNCP4 | DNCP3 | DNCP2 | DNCP1 | DNCP0 |
| Reset Value |     |     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                       |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                           |
| <b>DNCP[6:0]</b> | <b>NCP Clock Divider</b><br>These bits set the source clock divider value for the CP clock. These bits are ignored in clock auto set mode.<br>Default value: 0000000<br>0000000: Divide by 1<br>0000001: Divide by 2<br>...<br>1111111: Divide by 128 |

**Page 0 / Register 30**

| Dec         | Hex | b7  | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-------|-------|-------|-------|-------|-------|-------|
| 30          | 1E  | RSV | DOSR6 | DOSR5 | DOSR4 | DOSR3 | DOSR2 | DOSR1 | DOSR0 |
| Reset Value |     |     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                        |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                            |
| <b>DOSR[6:0]</b> | <b>OSR Clock Divider</b><br>These bits set the source clock divider value for the OSR clock. These bits are ignored in clock auto set mode.<br>Default value: 0000000<br>0000000: Divide by 1<br>0000001: Divide by 2<br>...<br>1111111: Divide by 128 |

**Page 0 / Register 32**

| Dec         | Hex | b7  | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-------|-------|-------|-------|-------|-------|-------|
| 32          | 20  | RSV | DBCK6 | DBCK5 | DBCK4 | DBCK3 | DBCK2 | DBCK1 | DBCK0 |
| Reset Value |     |     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                  |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                      |
| <b>DBCK[6:0]</b> | <b>Master Mode BCK Divider</b><br>These bits set the SCK divider value to generate I <sup>2</sup> S master BCK clock.<br>Default value: 0000000<br>0000000: Divide by 1<br>0000001: Divide by 2<br>...<br>1111111: Divide by 128 |

**Page 0 / Register 33**

| Dec         | Hex | b7    | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| 33          | 21  | DLRK7 | DLRK6 | DLRK5 | DLRK4 | DLRK3 | DLRK2 | DLRK1 | DLRK0 |
| Reset Value |     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                      |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DLRK[7:0]</b> | <b>Master Mode LRCK Divider</b><br>These bits set the I <sup>2</sup> S master BCK clock divider value to generate I <sup>2</sup> S master LRCK clock.<br>Default value: 00000000<br>00000000: Divide by 1<br>00000001: Divide by 2<br>...<br>11111111: Divide by 256 |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**Page 0 / Register 34**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-----|-----|-------|-------|
| 34          | 22  | RSV | RSV | RSV | RSV | RSV | RSV | FSSP1 | FSSP0 |
| Reset Value |     |     |     |     | 0   |     |     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                           |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                               |
| <b>FSSP[1:0]</b> | <b>f<sub>s</sub> Speed Mode</b><br>These bits select the f <sub>s</sub> operation mode, which must be set according to the current audio sampling rate. These bits are ignored in clock auto set mode.<br>Default value: 00<br>00: Single speed (f <sub>s</sub> = 48 kHz) |

|  |                                                               |
|--|---------------------------------------------------------------|
|  | 01: Double speed ( $48 \text{ kHz} < f_s = 96 \text{ kHz}$ )  |
|  | 10: Quad speed ( $96 \text{ kHz} < f_s = 192 \text{ kHz}$ )   |
|  | 11: Octal speed ( $192 \text{ kHz} < f_s = 384 \text{ kHz}$ ) |

**Page 0 / Register 35**

| Dec         | Hex | b7     | b6     | b5     | b4     | b3     | b2     | b1    | b0    |
|-------------|-----|--------|--------|--------|--------|--------|--------|-------|-------|
| 35          | 23  | IDAC15 | IDAC14 | IDAC13 | IDAC12 | IDAC11 | IDAC10 | IDAC9 | IDAC8 |
| Reset Value |     | 0      | 0      | 0      | 0      | 0      | 0      | 0     | 1     |

**Page 0 / Register 36**

| 36          | 24 | IDAC7 | IDAC6 | IDAC5 | IDAC4 | IDAC3 | IDAC2 | IDAC1 | IDAC0 |
|-------------|----|-------|-------|-------|-------|-------|-------|-------|-------|
| Reset Value |    | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

|                   |                                                                                                                                                                                                                                          |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>IDAC[15:0]</b> | <b>IDAC (MSB)</b><br>These bits specify the number of DSP clock cycles available in one audio frame. The value should match the DSP clock $f_s$ ratio. These bits are ignored in clock auto set mode.<br>Default value: 0000000100000000 |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**Page 0 / Register 37**

| Dec         | Hex | b7  | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
|-------------|-----|-----|------|------|------|------|------|------|------|
| 37          | 25  | RSV | IDFS | IDBK | IDSK | IDCH | IDCM | DCAS | IPLK |
| Reset Value |     |     | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

|             |                                                                                                                                                                                                                                                                                                                                  |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                      |
| <b>IDFS</b> | <b>Ignore <math>f_s</math> Detection</b><br>This bit controls whether to ignore the $f_s$ detection. When ignored, $f_s$ error will not cause a clock error.<br>Default value: 0<br>0: Regard $f_s$ detection<br>1: Ignore $f_s$ detection                                                                                       |
| <b>IDBK</b> | <b>Ignore BCK Detection</b><br>This bit controls whether to ignore the BCK detection against LRCK. The BCK must be stable between $32f_s$ and $256f_s$ inclusive or an error will be reported. When ignored, a BCK error will not cause a clock error.<br>Default value: 0<br>0: Regard BCK detection<br>1: Ignore BCK detection |
| <b>IDSK</b> | <b>Ignore SCK Detection</b><br>This bit controls whether to ignore the SCK detection against LRCK. Only some certain SCK ratios within some error margin are allowed. When ignored, an SCK error will not cause a clock error.<br>Default value: 0<br>0: Regard SCK detection<br>1: Ignore SCK detection                         |
| <b>IDCH</b> | <b>Ignore Clock Halt Detection</b><br>This bit controls whether to ignore the SCK halt (static or frequency is lower than acceptable) detection. When ignored an SCK halt will not cause a clock error.<br>Default value: 0<br>0: Regard SCK halt detection<br>1: Ignore SCK halt detection                                      |
| <b>IDCM</b> | <b>Ignore LRCK or BCK Missing Detection</b>                                                                                                                                                                                                                                                                                      |

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             | <p>This bit controls whether to ignore the LRCK or BCK missing detection. The LRCK or BCK need to be in low state (not only static) to be deemed missing. When ignored an LRCK or BCK missing will not cause the DAC go into powerdown mode.</p> <p>Default value: 0</p> <p>0: Regard LRCK or BCK missing detection</p> <p>1: Ignore LRCK or BCK missing detection</p>                                                                                                                                                                                                            |
| <b>DCAS</b> | <p><b>Disable Clock Divider Autoselect</b></p> <p>This bit enables or disables the clock auto set mode. When dealing with uncommon audio clock configuration, the auto set mode must be disabled and all clock dividers must be set manually. Additionally, some clock detectors might also need to be disabled. The clock autoselect feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled and the clock dividers must be set manually.</p> <p>Default value: 0</p> <p>0: Enable clock auto set</p> <p>1: Disable clock auto set</p> |
| <b>IPLK</b> | <p><b>Ignore PLL Lock Detection</b></p> <p>This bit controls whether to ignore the PLL lock detection. When ignored, PLL unlocks will not cause a clock error. The PLL lock flag at Page 0 / Register 4, bit 4 is always correct regardless of this bit.</p> <p>Default value: 0</p> <p>0: PLL unlocks raise clock error</p> <p>1: PLL unlocks are ignored</p>                                                                                                                                                                                                                    |

**Page 0 / Register 40**

| Dec         | Hex | b7  | b6  | b5    | b4    | b3  | b2  | b1    | b0    |
|-------------|-----|-----|-----|-------|-------|-----|-----|-------|-------|
| 40          | 28  | RSV | RSV | AFMT1 | AFMT0 | RSV | RSV | ALEN1 | ALEN0 |
| Reset Value |     |     |     | 0     | 0     |     |     | 1     | 0     |

|                  |                                                                                                                                                                                                                                                      |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <p><b>Reserved</b></p> <p>Reserved. Do not access.</p>                                                                                                                                                                                               |
| <b>AFMT[1:0]</b> | <p><b>I<sup>2</sup>S Data Format</b></p> <p>These bits control both input and output audio interface formats for DAC operation.</p> <p>Default value: 00</p> <p>00: I<sup>2</sup>S</p> <p>01: DSP</p> <p>10: RTJ</p> <p>11: LTJ</p>                  |
| <b>ALEN[1:0]</b> | <p><b>I<sup>2</sup>S Word Length</b></p> <p>These bits control both input and output audio interface sample word lengths for DAC operation.</p> <p>Default value: 10</p> <p>00: 16 bits</p> <p>01: 20 bits</p> <p>10: 24 bits</p> <p>11: 32 bits</p> |

**Page 0 / Register 41**

| Dec         | Hex | b7    | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| 41          | 29  | AOFS7 | AOFS6 | AOFS5 | AOFS4 | AOFS3 | AOFS2 | AOFS1 | AOFS0 |
| Reset Value |     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                   |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>AOFS[7:0]</b> | <p><b>I<sup>2</sup>S Shift</b></p> <p>These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio sample.</p> <p>Default value: 00000000</p> |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

|  |                                      |
|--|--------------------------------------|
|  | 00000000: offset = 0 BCK (no offset) |
|  | 00000001: ofset = 1 BCK              |
|  | 00000010: offset = 2 BCKs            |
|  |                                      |
|  | 11111111: offset = 256 BCKs          |

**Page 0 / Register 42**

| Dec         | Hex | b7  | b6  | b5    | b4    | b3  | b2  | b1    | b0    |
|-------------|-----|-----|-----|-------|-------|-----|-----|-------|-------|
| 42          | 2A  | RSV | RSV | AUPL1 | AUPL0 | RSV | RSV | AUPR1 | AUPR0 |
| Reset Value |     |     |     | 0     | 1     |     |     | 0     | 1     |

|                  |                                                                                                                                                                                                                             |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                 |
| <b>AUPL[1:0]</b> | <b>Left DAC Data Path</b><br>These bits control the left channel audio data path connection.<br>Default value: 01<br>00: Zero data (mute)<br>01: Left channel data<br>10: Right channel data<br>11: Reserved (do not set)   |
| <b>AUPR[1:0]</b> | <b>Right DAC Data Path</b><br>These bits control the right channel audio data path connection.<br>Default value: 01<br>00: Zero data (mute)<br>01: Right channel data<br>10: Left channel data<br>11: Reserved (do not set) |

**Page 0 / Register 43**

| Dec         | Hex | b7  | b6  | b5  | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-----|-------|-------|-------|-------|-------|
| 43          | 2B  | RSV | RSV | RSV | PSEL4 | PSEL3 | PSEL2 | PSEL1 | PSEL0 |
| Reset Value |     |     |     |     | 0     | 0     | 0     | 0     | 1     |

|                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <b>PSEL[4:0]</b> | <b>DSP Program Selection</b><br>These bits select the DSP program to use for audio processing.<br>Default value: 00001<br>00000: Reserved (do not set)<br>00001: 8x/4x/2x FIR interpolation filter with de-emphasis<br>00010: 8x/4x/2x Low latency IIR interpolation filter with de-emphasis<br>00011: High attenuation x8/x4/x2 interpolation filter with de-emphasis<br>00100: Reserved<br>00101: Fixed process flow with configurable parameters<br>00110: Reserved (do not set)<br>00111: 8x Ringing-less low latency FIR interpolation filter without de-emphasis<br>others: Reserved (do not set) |

**Page 0 / Register 44**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2    | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-----|-------|-------|-------|
| 44          | 2C  | RSV | RSV | RSV | RSV | RSV | CMDP2 | CMDP1 | CMDP0 |
| Reset Value |     |     |     |     |     |     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                           |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                               |
| <b>CMDP[2:0]</b> | <b>Clock Missing Detection Period</b><br>These bits set how long both BCK and LRCK keep low before the audio clocks deemed missing and the DAC transitions to powerdown mode.<br>Default value: 000<br>000: about 1 second<br>001: about 2 seconds<br>010: about 3 seconds<br>...<br>111: about 8 seconds |

**Page 0 / Register 59**

| Dec         | Hex | b7  | b6    | b5    | b4    | b3  | b2    | b1    | b0    |
|-------------|-----|-----|-------|-------|-------|-----|-------|-------|-------|
| 59          | 3B  | RSV | AMTL2 | AMTL1 | AMTL0 | RSV | AMTR2 | AMTR1 | AMTR0 |
| Reset Value |     |     | 0     | 0     | 0     |     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                     |
| <b>AMTL[2:0]</b> | <b>Auto Mute Time for Left Channel</b><br>These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 48 kHz sampling rate and will scale with other rates.<br>Default value: 000<br>000: 21 ms<br>001: 106 ms<br>010: 213 ms<br>011: 533 ms<br>100: 1.07 sec<br>101: 2.13 sec<br>110: 5.33 sec<br>111: 10.66 sec   |
| <b>AMTR[2:0]</b> | <b>Auto Mute Time for Right Channel</b><br>These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 48 kHz sampling rate and will scale with other rates.<br>Default value: 000<br>000: 21 ms<br>001: 106 ms<br>010: 213 ms<br>011: 533 ms<br>100: 1.07 sec<br>101: 2.13 sec<br>110: 5.33 sec<br>111: 10.66 sec |

**Page 0 / Register 60**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-----|-----|-------|-------|
| 60          | 3C  | RSV | RSV | RSV | RSV | RSV | RSV | PCTL1 | PCTL0 |
| Reset Value |     |     |     |     |     |     |     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                                                                       |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                           |
| <b>PCTL[1:0]</b> | <b>Digital Volume Control</b><br>These bits control the behavior of the digital volume.<br>Default value: 00<br>00: The volume for Left and right channels are independent<br>01: Right channel volume follows left channel setting<br>10: Left channel volume follows right channel setting<br>11: Reserved (The volume for Left and right channels are independent) |

**Page 0 / Register 61**

| Dec         | Hex | b7    | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| 61          | 3D  | VOLL7 | VOLL6 | VOLL5 | VOLL4 | VOLL3 | VOLL2 | VOLL1 | VOLL0 |
| Reset Value |     | 0     | 0     | 1     | 1     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                              |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>VOLL[7:0]</b> | <b>Left Digital Volume</b><br>These bits control the left channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step.<br>Default value: 00110000<br>00000000: +24.0 dB<br>00000001: +23.5 dB<br>00101111: +0.5 dB<br>00110000: 0.0 dB<br>00110001: -0.5 dB<br>...<br>11111110: -103 dB<br>11111111: Mute |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**Page 0 / Register 62**

| Dec         | Hex | b7    | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| 62          | 3E  | VOLR7 | VOLR6 | VOLR5 | VOLR4 | VOLR3 | VOLR2 | VOLR1 | VOLR0 |
| Reset Value |     | 0     | 0     | 1     | 1     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                                |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>VOLR[7:0]</b> | <b>Right Digital Volume</b><br>These bits control the right channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step.<br>Default value: 00110000<br>00000000: +24.0 dB<br>00000001: +23.5 dB<br>00101111: +0.5 dB<br>00110000: 0.0 dB<br>00110001: -0.5 dB<br>...<br>11111110: -103 dB<br>11111111: Mute |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**Page 0 / Register 63**

| Dec         | Hex | b7    | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| 63          | 3F  | VNDF1 | VNDF0 | VNDS1 | VNDS0 | VNUF1 | VNUF0 | VNUS1 | VNUS0 |
| Reset Value |     | 0     | 0     | 1     | 0     | 0     | 0     | 1     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>VNDF[1:0]</b> | <b>Digital Volume Normal Ramp Down Frequency</b><br>These bits control the frequency of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by XSMUTE pin or Page 0 / Register 3.<br>Default value: 00<br>00: Update every 1 sample period<br>01: Update every 2 sample periods<br>10: Update every 4 sample periods<br>11: Directly set the volume to zero (Instant mute) |
| <b>VNDS[1:0]</b> | <b>Digital Volume Normal Ramp Down Step</b><br>These bits control the step of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by XSMUTE pin or Page 0 / Register 3.<br>Default value: 10<br>00: Decrement by 4 dB for each update<br>01: Decrement by 2 dB for each update<br>10: Decrement by 1 dB for each update<br>11: Decrement by 0.5 dB for each update         |
| <b>VNUF[1:0]</b> | <b>Digital Volume Normal Ramp Up Frequency</b><br>These bits control the frequency of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by XSMUTE pin or Page 0 / Register 3.<br>Default value: 00<br>00: Update every 1 sample period<br>01: Update every 2 sample periods<br>10: Update every 4 sample periods<br>11: Directly restore the volume (Instant unmute)     |
| <b>VNUS[1:0]</b> | <b>Digital Volume Normal Ramp Up Step</b><br>These bits control the step of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by XSMUTE pin or Page 0 / Register 3.<br>Default value: 10<br>00: Increment by 4 dB for each update<br>01: Increment by 2 dB for each update<br>10: Increment by 1 dB for each update<br>11: Increment by 0.5 dB for each update           |

**Page 0 / Register 64**

| Dec         | Hex | b7    | b6    | b5    | b4    | b3  | b2  | b1  | b0  |
|-------------|-----|-------|-------|-------|-------|-----|-----|-----|-----|
| 64          | 40  | VEDF1 | VEDF0 | VEDS1 | VEDS0 | RSV | RSV | RSV | RSV |
| Reset Value |     | 0     | 0     | 0     | 0     |     |     |     |     |

|                  |                                                                                                                                                                                                                                                                                                                                                            |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                |
| <b>VEDF[1:0]</b> | <b>Digital Volume Emergency Ramp Down Frequency</b><br>These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute.<br>Default value: 00<br>00: Update every 1 sample period<br>01: Update every 2 sample periods |

|                  |                                                                                                                                                                                                                                                                                                                                                           |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | 10: Update every 4 sample periods                                                                                                                                                                                                                                                                                                                         |
|                  | 11: Directly set the volume to zero (Instant mute)                                                                                                                                                                                                                                                                                                        |
| <b>VEDS[1:0]</b> | <b>Digital Volume Emergency Ramp Down Step</b><br>These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute.<br>Default value: 00<br>00: Decrement by 4 dB for each update<br>01: Decrement by 2 dB for each update |
|                  | 10: Decrement by 1 dB for each update                                                                                                                                                                                                                                                                                                                     |
|                  | 11: Decrement by 0.5 dB for each update                                                                                                                                                                                                                                                                                                                   |

### Page 0 / Register 65

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2   | b1   | b0   |
|-------------|-----|-----|-----|-----|-----|-----|------|------|------|
| 65          | 41  | RSV | RSV | RSV | RSV | RSV | ACTL | AMLE | AMRE |
| Reset Value |     |     |     |     |     |     | 1    | 1    | 1    |

|             |                                                                                                                                                                                                                                                                                                                                                            |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                |
| <b>ACTL</b> | <b>Auto Mute Control</b><br>This bit controls the behavior of the auto mute upon zero sample detection. The time length for zero detection is set with Page 0 / Register 59.<br>Default value: 1<br>0: Auto mute left channel and right channel independently.<br>1: Auto mute left and right channels only when both channels are about to be auto muted. |
| <b>AMLE</b> | <b>Auto Mute Left Channel</b><br>This bit enables or disables auto mute on right channel. Note that when right channel auto mute is disabled and the Page 0 / Register 65, bit 2 is set to 1, the left channel will also never be auto muted.<br>Default value: 1<br>0: Disable right channel auto mute<br>1: Enable right channel auto mute               |
| <b>AMRE</b> | <b>Auto Mute Right Channel</b><br>This bit enables or disables auto mute on left channel. Note that when left channel auto mute is disabled and the Page 0 / Register 65, bit 2 is set to 1, the right channel will also never be auto muted.<br>Default value: 1<br>0: Disable left channel auto mute<br>1: Enable left channel auto mute                 |

### Page 0 / Register 80

| Dec         | Hex | b7  | b6  | b5  | b4  | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-------|-------|-------|-------|
| 80          | 50  | RSV | RSV | RSV | RSV | G1SL3 | G1SL2 | G1SL1 | G1SL0 |
| Reset Value |     |     |     |     |     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                         |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                             |
| <b>G1SL[3:0]</b> | <b>GPIO1 Output Selection</b><br>These bits select the signal to output to GPIO1. To actually output the selected signal, the GPIO1 must be set to output mode at Page 0 / Register 8.<br>Default value: 0000<br>0000: off (low)<br>0001: DSP GPIO1 output<br>0010: Register GPIO1 output (Page 0 / Register 86, bit 0) |

|  |                                                                                |
|--|--------------------------------------------------------------------------------|
|  | 0011: Auto mute flag (asserted when both L and R channels are auto muted)      |
|  | 0100: Auto mute flag for left channel                                          |
|  | 0101: Auto mute flag for right channel                                         |
|  | 0110: Clock invalid flag (clock error or clock changing or clock missing)      |
|  | 0111: Serial audio interface data output (SDOUT)                               |
|  | 1000: Analog mute flag for left channel (low active)                           |
|  | 1001: Analog mute flag for right channel (low active)                          |
|  | 1010: PLL lock flag                                                            |
|  | 1011: Charge pump clock                                                        |
|  | 1100: Reserved                                                                 |
|  | 1101: Reserved                                                                 |
|  | 1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD |
|  | 1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD |

**Page 0 / Register 81**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-------|-------|-------|-------|
| 81          | 51  | RSV | RSV | RSV | RSV | G2SL3 | G2SL2 | G2SL1 | G2SL0 |
| Reset Value |     |     |     |     |     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>G2SL[3:0]</b> | <b>GPIO2 Output Selection</b><br>These bits select the signal to output to GPIO2. To actually output the selected signal, the GPIO2 must be set to output mode at Page 0 / Register 8.<br>Default value: 0000<br>0000: off (low)<br>0001: DSP GPIO2 output<br>0010: Register GPIO2 output (Page 0 / Register 86, bit 1)<br>0011: Auto mute flag (asserted when both L and R channels are auto muted)<br>0100: Auto mute flag for left channel<br>0101: Auto mute flag for right channel<br>0110: Clock invalid flag (clock error or clock changing or clock missing)<br>0111: Serial audio interface data output (SDOUT)<br>1000: Analog mute flag for left channel (low active)<br>1001: Analog mute flag for right channel (low active)<br>1010: PLL lock flag<br>1011: Charge pump clock<br>1100: Reserved<br>1101: Reserved<br>1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD<br>1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD |

**Page 0 / Register 82**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-------|-------|-------|-------|
| 82          | 52  | RSV | RSV | RSV | RSV | G3SL3 | G3SL2 | G3SL1 | G3SL0 |
| Reset Value |     |     |     |     |     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>G3SL[3:0]</b> | <b>GPIO3 Output Selection</b><br>These bits select the signal to output to GPIO3. To actually output the selected signal, the GPIO3 must be set to output mode at Page 0 / Register 8.<br>Default value: 0000<br>0000: off (low)<br>0001: DSP GPIO3 output<br>0010: Register GPIO3 output (Page 0 / Register 86, bit 2)<br>0011: Auto mute flag (asserted when both L and R channels are auto muted)<br>0100: Auto mute flag for left channel<br>0101: Auto mute flag for right channel<br>0110: Clock invalid flag (clock error or clock changing or clock missing)<br>0111: Serial audio interface data output (SDOUT)<br>1000: Analog mute flag for left channel (low active)<br>1001: Analog mute flag for right channel (low active)<br>1010: PLL lock flag<br>1011: Charge pump clock<br>1100: Reserved<br>1101: Reserved<br>1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD<br>1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD |

**Page 0 / Register 83**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-------|-------|-------|-------|
| 83          | 53  | RSV | RSV | RSV | RSV | G4SL3 | G4SL2 | G4SL1 | G4SL0 |
| Reset Value |     |     |     |     |     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>G4SL[3:0]</b> | <b>GPIO4 Output Selection</b><br>These bits select the signal to output to GPIO4. To actually output the selected signal, the GPIO4 must be set to output mode at Page 0 / Register 8.<br>Default value: 0000<br>0000: off (low)<br>0001: DSP GPIO4 output<br>0010: Register GPIO4 output (Page 0 / Register 86, bit 3)<br>0011: Auto mute flag (asserted when both L and R channels are auto muted)<br>0100: Auto mute flag for left channel<br>0101: Auto mute flag for right channel<br>0110: Clock invalid flag (clock error or clock changing or clock missing)<br>0111: Serial audio interface data output (SDOUT)<br>1000: Analog mute flag for left channel (low active)<br>1001: Analog mute flag for right channel (low active)<br>1010: PLL lock flag<br>1011: Charge pump clock<br>1100: Reserved<br>1101: Reserved<br>1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD<br>1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD |

**Page 0 / Register 84**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-------|-------|-------|-------|
| 84          | 54  | RSV | RSV | RSV | RSV | G5SL3 | G5SL2 | G5SL1 | G5SL0 |
| Reset Value |     |     |     |     |     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>G5SL[3:0]</b> | <b>GPIO5 Output Selection</b><br>These bits select the signal to output to GPIO5. To actually output the selected signal, the GPIO5 must be set to output mode at Page 0 / Register 8.<br>Default value: 0000<br>0000: off (low)<br>0001: DSP GPIO5 output<br>0010: Register GPIO5 output (Page 0 / Register 86, bit 4)<br>0011: Auto mute flag (asserted when both L and R channels are auto muted)<br>0100: Auto mute flag for left channel<br>0101: Auto mute flag for right channel<br>0110: Clock invalid flag (clock error or clock changing or clock missing)<br>0111: Serial audio interface data output (SDOUT)<br>1000: Analog mute flag for left channel (low active)<br>1001: Analog mute flag for right channel (low active)<br>1010: PLL lock flag<br>1011: Charge pump clock<br>1100: Reserved<br>1101: Reserved<br>1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD<br>1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD |

**Page 0 / Register 85**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-----|-----|-------|-------|-------|-------|
| 85          | 55  | RSV | RSV | RSV | RSV | G6SL3 | G6SL2 | G6SL1 | G6SL0 |
| Reset Value |     |     |     |     |     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>G6SL[3:0]</b> | <b>GPIO6 Output Selection</b><br>These bits select the signal to output to GPIO6. To actually output the selected signal, the GPIO6 must be set to output mode at Page 0 / Register 8.<br>Default value: 0000<br>0000: off (low)<br>0001: DSP GPIO6 output<br>0010: Register GPIO6 output (Page 0 / Register 86, bit 5)<br>0011: Auto mute flag (asserted when both L and R channels are auto muted)<br>0100: Auto mute flag for left channel<br>0101: Auto mute flag for right channel<br>0110: Clock invalid flag (clock error or clock changing or clock missing)<br>0111: Serial audio interface data output (SDOUT)<br>1000: Analog mute flag for left channel (low active)<br>1001: Analog mute flag for right channel (low active)<br>1010: PLL lock flag |

|  |                                                                                |
|--|--------------------------------------------------------------------------------|
|  | 1011: Charge pump clock                                                        |
|  | 1100: Reserved                                                                 |
|  | 1101: Reserved                                                                 |
|  | 1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD |
|  | 1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD |
|  |                                                                                |

**Page 0 / Register 86**

| Dec         | Hex | b7  | b6  | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-------|-------|-------|-------|-------|-------|
| 86          | 56  | RSV | RSV | GOUT5 | GOUT4 | GOUT3 | GOUT2 | GOUT1 | GOUT0 |
| Reset Value |     |     |     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                          |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                              |
| <b>GOUT[5:0]</b> | <b>GPIO Output Control</b><br>This bit controls the GPIO6 output when the selection at Page 0 / Register 85 is set to 0010 (register output)<br>Default value: 000000<br>0: Output low<br>1: Output high |

**Page 0 / Register 87**

| Dec         | Hex | b7  | b6  | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-----|-------|-------|-------|-------|-------|-------|
| 87          | 57  | RSV | RSV | GINV5 | GINV4 | GINV3 | GINV2 | GINV1 | GINV0 |
| Reset Value |     |     |     | 0     | 0     | 0     | 0     | 0     | 0     |

|                  |                                                                                                                                                                                                                      |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                          |
| <b>GINV[5:0]</b> | <b>GPIO Output Inversion</b><br>This bit controls the polarity of GPIO6 output. When set to 1, the output will be inverted for any signal being selected.<br>Default value: 000000<br>0: Non-inverted<br>1: Inverted |

**Page 0 / Register 90**

| Dec         | Hex | b7  | b6  | b5  | b4   | b3   | b2   | b1   | b0   |
|-------------|-----|-----|-----|-----|------|------|------|------|------|
| 90          | 5A  | RSV | RSV | RSV | L1OV | R1OV | L2OV | R2OV | SFOV |
| Reset Value |     |     |     |     |      |      |      |      |      |

|             |                                                                                                                                                                                                              |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                  |
| <b>L1OV</b> | <b>Left1 Overflow (Read Only)</b><br>This bit indicates whether the left channel of DSP first output port has overflow. This bit is sticky and is cleared when read. 0: No overflow<br>1: Overflow occurred  |
| <b>R1OV</b> | <b>Right1 Overflow (Read Only)</b><br>The bit indicates whether the right channel of DSP first output port has overflow. This bit is sticky and is cleared when read. 0: No overflow<br>1: Overflow occurred |
| <b>L2OV</b> | <b>Left2 Overflow (Read Only)</b><br>This bit indicates whether the left channel of DSP second output port has overflow. This bit is sticky and is cleared when read. 0: No overflow                         |

|             |                                                                                                                                                                                                                          |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             | 1: Overflow occurred                                                                                                                                                                                                     |
| <b>R2OV</b> | <b>Right2 Overflow (Read Only)</b><br>The bit indicates whether the right channel of DSP second output port has overflow. This bit is sticky and is cleared when read. 0: No overflow<br>1: Overflow occurred            |
| <b>SFOV</b> | <b>Shifter Overflow (Read Only)</b><br>This bit indicates whether overflow occurred in the DSP shifter (possible sample corruption). This bit is sticky and is cleared when read. 0: No overflow<br>1: Overflow occurred |

## Page 0 / Register 91

| Dec         | Hex | b7  | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-------|-------|-------|-------|-------|-------|-------|
| 91          | 5B  | RSV | DTFS2 | DTFS1 | DTFS0 | DTSR3 | DTSR2 | DTSR1 | DTSR0 |
| Reset Value |     |     |       |       |       |       |       |       |       |

|                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <b>DTFS[2:0]</b> | <b>Detected <math>f_s</math> (Read Only)</b><br>These bits indicate the currently detected audio sampling rate. 000: Error (Out of valid range)<br>001: 8 kHz<br>010: 16 kHz<br>011: 32-48 kHz<br>100: 88.2-96 kHz<br>101: 176.4-192 kHz<br>110: 384 kHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>DTSR[3:0]</b> | <b>Detected SCK Ratio (Read Only)</b><br>These bits indicate the currently detected SCK ratio. Note that even if the SCK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the SCK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute SCK frequency must also be lower than 50 MHz. 0000: Ratio error (The SCK ratio is not allowed)<br>0001: SCK = $32f_s$<br>0010: SCK = $48f_s$<br>0011: SCK = $64f_s$<br>0100: SCK = $128f_s$<br>0101: SCK = $192f_s$<br>0110: SCK = $256f_s$<br>0111: SCK = $384f_s$<br>1000: SCK = $512f_s$<br>1001: SCK = $768f_s$<br>1010: SCK = $1024f_s$<br>1011: SCK = $1152f_s$<br>1100: SCK = $1536f_s$<br>1101: SCK = $2048f_s$<br>1110: SCK = $3072f_s$ |

## Page 0 / Register 92

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0    |
|-------------|-----|-----|-----|-----|-----|-----|-----|-----|-------|
| 92          | 5C  | RSV | RSV | RSV | RSV | RSV | RSV | RSV | DTBR8 |
| Reset Value |     |     |     |     |     |     |     |     |       |

**Page 0 / Register 93**

| 93          | 5D | DTBR7 | DTBR6 | DTBR5 | DTBR4 | DTBR3 | DTBR2 | DTBR1 | DTBR0 |
|-------------|----|-------|-------|-------|-------|-------|-------|-------|-------|
| Reset Value |    |       |       |       |       |       |       |       |       |

|                  |                                                                                                                                                                                                                                                                                     |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                         |
| <b>DTBR[8:0]</b> | <b>Detected BCK Ratio (MSB) (Read Only)</b><br>These bits indicate the currently detected BCK ratio, that is, the number of BCK clocks in one audio frame. Note that for the extreme case of BCK = 1 f <sub>S</sub> (not a usable scenario), the detected ratio will be unreliable. |

**Page 0 / Register 94**

| Dec         | Hex | b7  | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
|-------------|-----|-----|-------|-------|-------|-------|-------|-------|-------|
| 94          | 5E  | RSV | CDST6 | CDST5 | CDST4 | CDST3 | CDST2 | CDST1 | CDST0 |
| Reset Value |     |     |       |       |       |       |       |       |       |

|                  |                                                                                                                                                         |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                                                             |
| <b>CDST[6:0]</b> | <b>Clock Detector Status (Read Only)</b><br>This bit indicates whether the SCK clock is present or not. 0: SCK is present<br>1: SCK is missing (halted) |

**Page 0 / Register 108**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1   | b0   |
|-------------|-----|-----|-----|-----|-----|-----|-----|------|------|
| 108         | 6C  | RSV | RSV | RSV | RSV | RSV | RSV | AMLM | AMRM |
| Reset Value |     |     |     |     |     |     |     |      |      |

|             |                                                                                                                                  |
|-------------|----------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                      |
| <b>AMLM</b> | <b>Left Analog Mute Monitor (Read Only)</b><br>This bit is a monitor for left channel analog mute status. 0: Mute<br>1: Unmute   |
| <b>AMRM</b> | <b>Right Analog Mute Monitor (Read Only)</b><br>This bit is a monitor for right channel analog mute status. 0: Mute<br>1: Unmute |

**Page 0 / Register 119**

| Dec         | Hex | b7  | b6  | b5    | b4    | b3    | b2    | b1    | b0  |
|-------------|-----|-----|-----|-------|-------|-------|-------|-------|-----|
| 119         | 77  | RSV | RSV | GPIN5 | GPIN4 | GPIN3 | GPIN2 | GPIN1 | RSV |
| Reset Value |     |     |     |       |       |       |       |       |     |

|                  |                                                                                                            |
|------------------|------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>       | <b>Reserved</b><br>Reserved. Do not access.                                                                |
| <b>GPIN[5:0]</b> | <b>GPIO Input States (Read Only)</b><br>This bit indicates the logic level at GPIO6 pin. 0: Low<br>1: High |

**Page 0 / Register 120**

| Dec         | Hex | b7  | b6  | b5  | b4   | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|------|-----|-----|-----|------|
| 120         | 78  | RSV | RSV | RSV | AMFL | RSV | RSV | RSV | AMFR |
| Reset Value |     |     |     |     |      |     |     |     |      |

|             |                                                                                                                                                      |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                          |
| <b>AMFL</b> | <b>Auto Mute Flag for Left Channel (Read Only)</b><br>This bit indicates the auto mute status for left channel. 0: Not auto muted<br>1: Auto muted   |
| <b>AMFR</b> | <b>Auto Mute Flag for Right Channel (Read Only)</b><br>This bit indicates the auto mute status for right channel. 0: Not auto muted<br>1: Auto muted |

**Page 1 / Register 1**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| 1           | 01  | RSV | RSV | RSV | RSV | RSV | RSV | RSV | OSEL |
| Reset Value |     |     |     |     |     |     |     |     | 0    |

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>OSEL</b> | <b>Output Amplitude Type</b><br>This bit selects the output amplitude type. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled via Page 0 / Register 37 and the clock dividers must be set manually.<br><br>Default value: 0<br>0: VREF mode (Constant output amplitude against AVDD variation)<br>1: VCOM mode (Output amplitude is proportional to AVDD variation) |

**Page 1 / Register 2**

| Dec         | Hex | b7  | b6  | b5  | b4   | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|------|-----|-----|-----|------|
| 2           | 02  | RSV | RSV | RSV | LAGN | RSV | RSV | RSV | RAGN |
| Reset Value |     |     |     |     | 0    |     |     |     | 0    |

|             |                                                                                                                                                 |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                     |
| <b>LAGN</b> | <b>Analog Gain Control for Left Channel</b><br>This bit controls the left channel analog gain.<br><br>Default value: 0<br>0: 0 dB<br>1: -6 dB   |
| <b>RAGN</b> | <b>Analog Gain Control for Right Channel</b><br>This bit controls the right channel analog gain.<br><br>Default value: 0<br>0: 0 dB<br>1: -6 dB |

**Page 1 / Register 5**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1   | b0   |
|-------------|-----|-----|-----|-----|-----|-----|-----|------|------|
| 5           | 05  | RSV | RSV | RSV | RSV | RSV | RSV | UEPD | UIPD |
| Reset Value |     |     |     |     |     |     |     | 0    | 0    |

|             |                                                                                                                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                         |
| <b>UEPD</b> | <b>External UVP Control</b><br>This bit enables or disables detection of power supply drop via XSMUTE pin (External Under Voltage Protection).<br><br>Default value: 0<br>0: Enabled<br>1: Disabled |
| <b>UIPD</b> | <b>Internal UVP Control</b><br>This bit enables or disables internal detection of AVDD voltage drop (Internal Under Voltage Protection).<br><br>Default value: 0<br>0: Enabled<br>1: Disabled       |

**Page 1 / Register 6**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| 6           | 06  | RSV | RSV | RSV | RSV | RSV | RSV | RSV | AMCT |
| Reset Value |     |     |     |     |     |     |     |     | 0    |

|             |                                                                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                         |
| <b>AMCT</b> | <b>Analog Mute Control</b><br>This bit enables or disables analog mute following digital mute.<br><br>Default value: 0<br>0: Enabled<br>1: Disabled |

**Page 1 / Register 7**

| Dec         | Hex | b7  | b6  | b5  | b4   | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|------|-----|-----|-----|------|
| 7           | 07  | RSV | RSV | RSV | AGBL | RSV | RSV | RSV | AGBR |
| Reset Value |     |     |     |     | 0    |     |     |     | 0    |

|             |                                                                                                                                                                                                         |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                             |
| <b>AGBL</b> | <b>Analog +10% Gain for Left Channel</b><br>This bit enables or disables amplitude boost mode for left channel.<br><br>Default value: 0<br>0: Normal amplitude<br>1: +10% (+0.8 dB) boosted amplitude   |
| <b>AGBR</b> | <b>Analog +10% Gain for Right Channel</b><br>This bit enables or disables amplitude boost mode for right channel.<br><br>Default value: 0<br>0: Normal amplitude<br>1: +10% (+0.8 dB) boosted amplitude |

**Page 1 / Register 8**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| 8           | 08  | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RCMF |
| Reset Value |     |     |     |     |     |     |     |     | 0    |

|             |                                                                                                                                                                                                                              |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                  |
| <b>RCMF</b> | <b>VCOM Reference Ramp Up</b><br>This bit controls the VCOM voltage ramp up speed.<br>Default value: 0<br>0: Normal ramp up, ~600ms with external capacitance = 1uF<br>1: Fast ramp up, ~3ms with external capacitance = 1uF |

**Page 1 / Register 9**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0   |
|-------------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| 9           | 09  | RSV | RSV | RSV | RSV | RSV | RSV | RSV | VCPD |
| Reset Value |     |     |     |     |     |     |     |     | 1    |

|             |                                                                                                                                                        |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                            |
| <b>VCPD</b> | <b>Power down control for VCOM</b><br>This bit controls VCOM powerdown switch.<br>Default value: 1<br>0: VCOM is powered on<br>1: VCOM is powered down |

**Page 44 / Register 1**

| Dec         | Hex | b7  | b6  | b5  | b4  | b3   | b2   | b1   | b0   |
|-------------|-----|-----|-----|-----|-----|------|------|------|------|
| 1           | 01  | RSV | RSV | RSV | RSV | ACRM | AMDC | ACRS | ACSW |
| Reset Value |     |     |     |     |     |      | 0    |      | 0    |

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>RSV</b>  | <b>Reserved</b><br>Reserved. Do not access.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>ACRM</b> | <b>Active CRAM Monitor (Read Only)</b><br>This bit indicates which CRAM is being accessed by the DSP when adaptive mode is disabled. When adaptive mode is enabled, this bit has no meaning. 0: CRAM A is being used by the DSP<br>1: CRAM B is being used by the DSP                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <b>AMDC</b> | <b>Adaptive Mode Control</b><br>This bit controls the DSP adaptive mode. When in adaptive mode, only CRAM A is accessible via serial interface when the DSP is disabled (DAC in standby state), while when the DSP is enabled (DAC is run state) the CRAM A can only be accessed by the DSP and the CRAM B can only be accessed by the serial interface, or vice versa depending on the value of CRAMSTAT. When not in adaptive mode, both CRAM A and B can be accessed by the serial interface when the DSP is disabled, but when the DSP is enabled, no CRAM can be accessed by serial interface. The DSP can access either CRAM, which can be monitored at SWPMON.<br>Default value: 0<br>0: Adaptive mode disabled<br>1: Adaptive mode enabled |
| <b>ACRS</b> | <b>Active CRAM Selection (Read Only)</b><br>This bit indicates which CRAM currently serves as the active one. The other CRAM serves as an update buffer, and can accessed by serial interface (SPI or I2C) 0: CRAM A is active and being used by the DSP<br>1: CRAM B is active and being used by the DSP                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>ACSW</b> | <b>Switch Active CRAM</b><br>This bit is a role-switch request between the two buffers, switching the active buffer role between CRAM A and CRAM B. This bit clears automatically when the switching process completed.<br>Default value: 0<br>0: No switching requested or switching completed<br>1: Switching is being requested                                                                                                                                                                                                                                                                                                                                                                                                                 |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Samples<br>(Requires Login) |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|-----------------------------|
| PCM5121PW        | ACTIVE        | TSSOP        | PW                 | 28   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   |                             |
| PCM5121PWR       | ACTIVE        | TSSOP        | PW                 | 28   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   |                             |
| PCM5122PW        | ACTIVE        | TSSOP        | PW                 | 28   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   |                             |
| PCM5122PWR       | ACTIVE        | TSSOP        | PW                 | 28   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   |                             |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

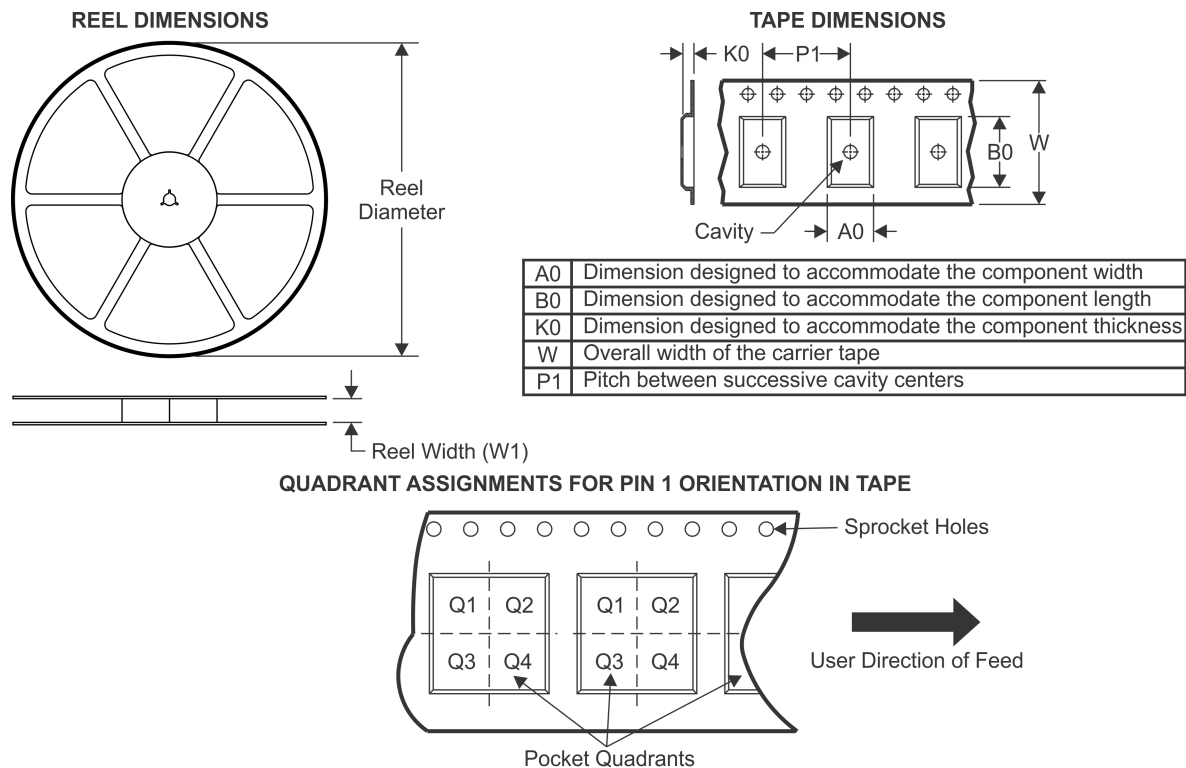
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

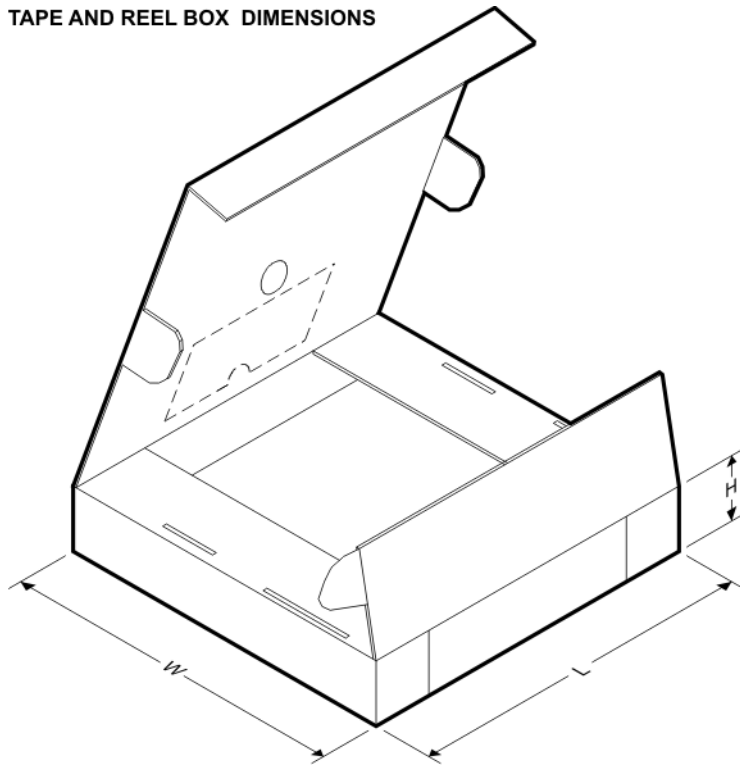
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCM5121PWR | TSSOP        | PW              | 28   | 2000 | 330.0              | 16.4               | 6.9     | 10.2    | 1.8     | 12.0    | 16.0   | Q1            |
| PCM5122PWR | TSSOP        | PW              | 28   | 2000 | 330.0              | 16.4               | 6.9     | 10.2    | 1.8     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

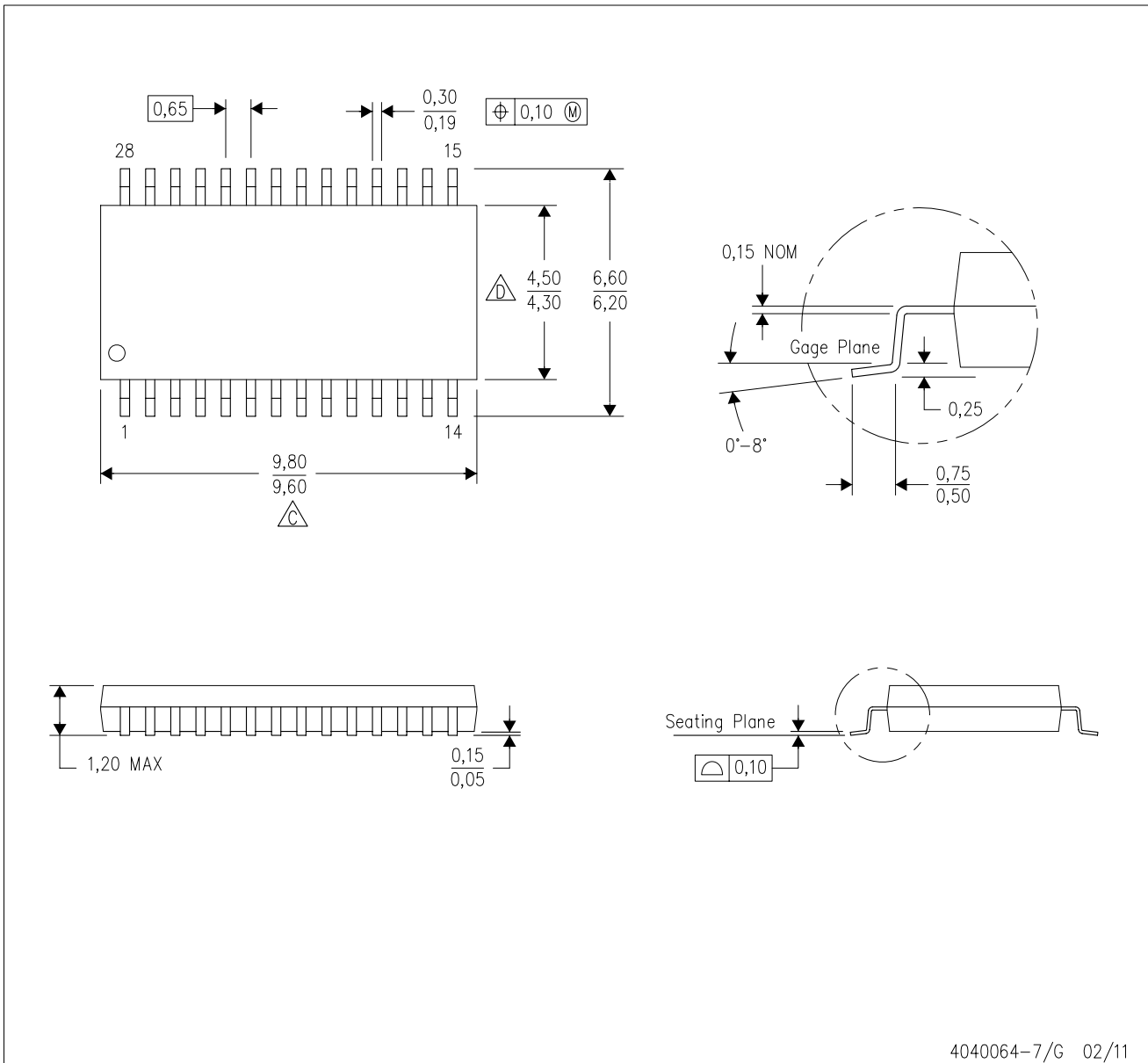


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCM5121PWR | TSSOP        | PW              | 28   | 2000 | 367.0       | 367.0      | 38.0        |
| PCM5122PWR | TSSOP        | PW              | 28   | 2000 | 367.0       | 367.0      | 38.0        |

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

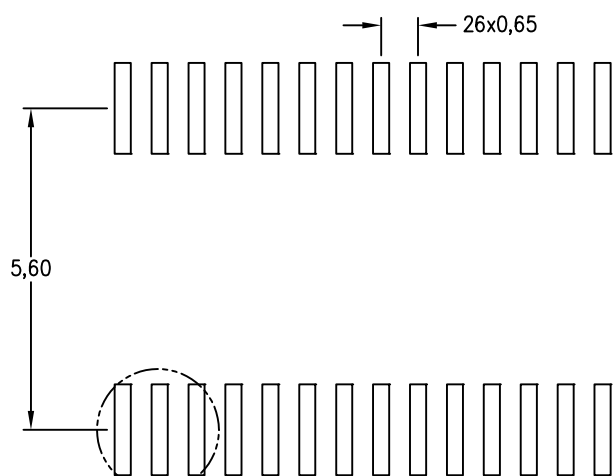


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

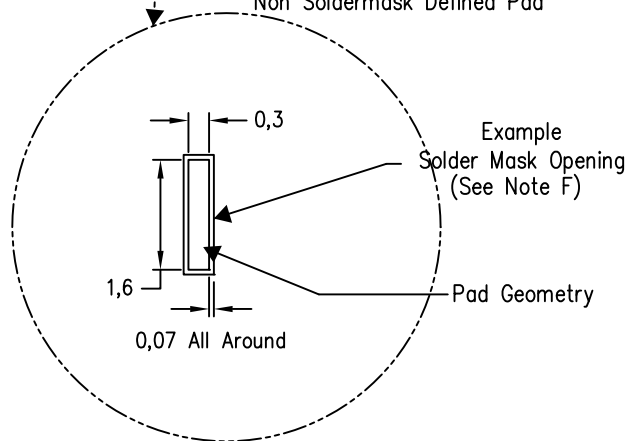
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

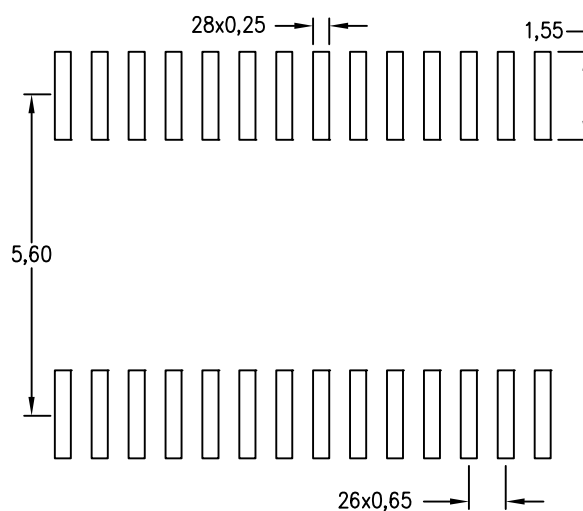
Example Board Layout



Example  
Non Soldermask Defined Pad



Stencil Openings  
Based on a stencil thickness  
of .127mm (.005inch).



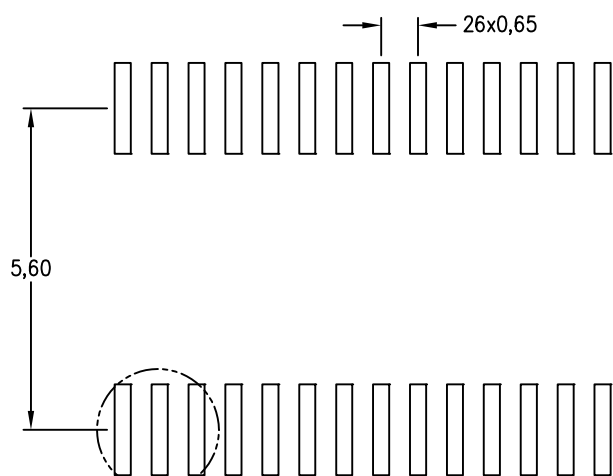
4211284-6/F 12/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate design.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

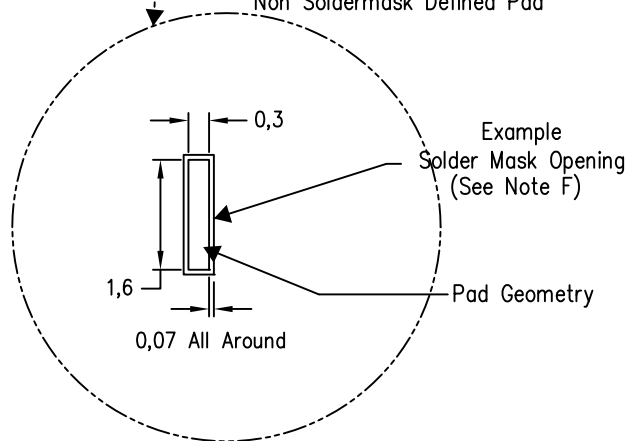
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

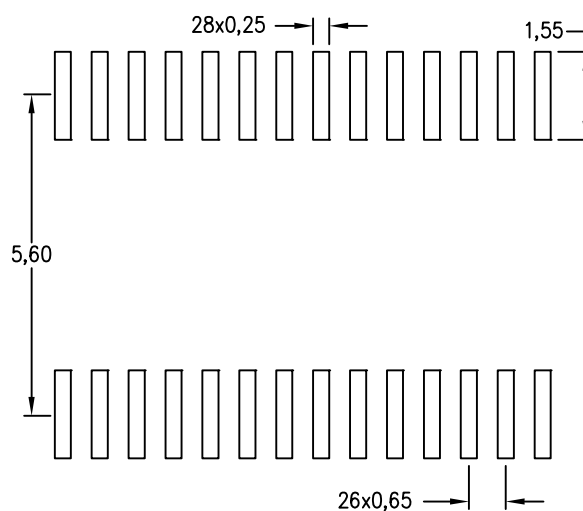
Example Board Layout



Example  
Non Soldermask Defined Pad



Stencil Openings  
Based on a stencil thickness  
of .127mm (.005inch).



4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

|                              |                                                                                      |
|------------------------------|--------------------------------------------------------------------------------------|
| Audio                        | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                               |
| Amplifiers                   | <a href="http://amplifier.ti.com">amplifier.ti.com</a>                               |
| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>                                         |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>                                           |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |                                                                                          |
|-------------------------------|------------------------------------------------------------------------------------------|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)